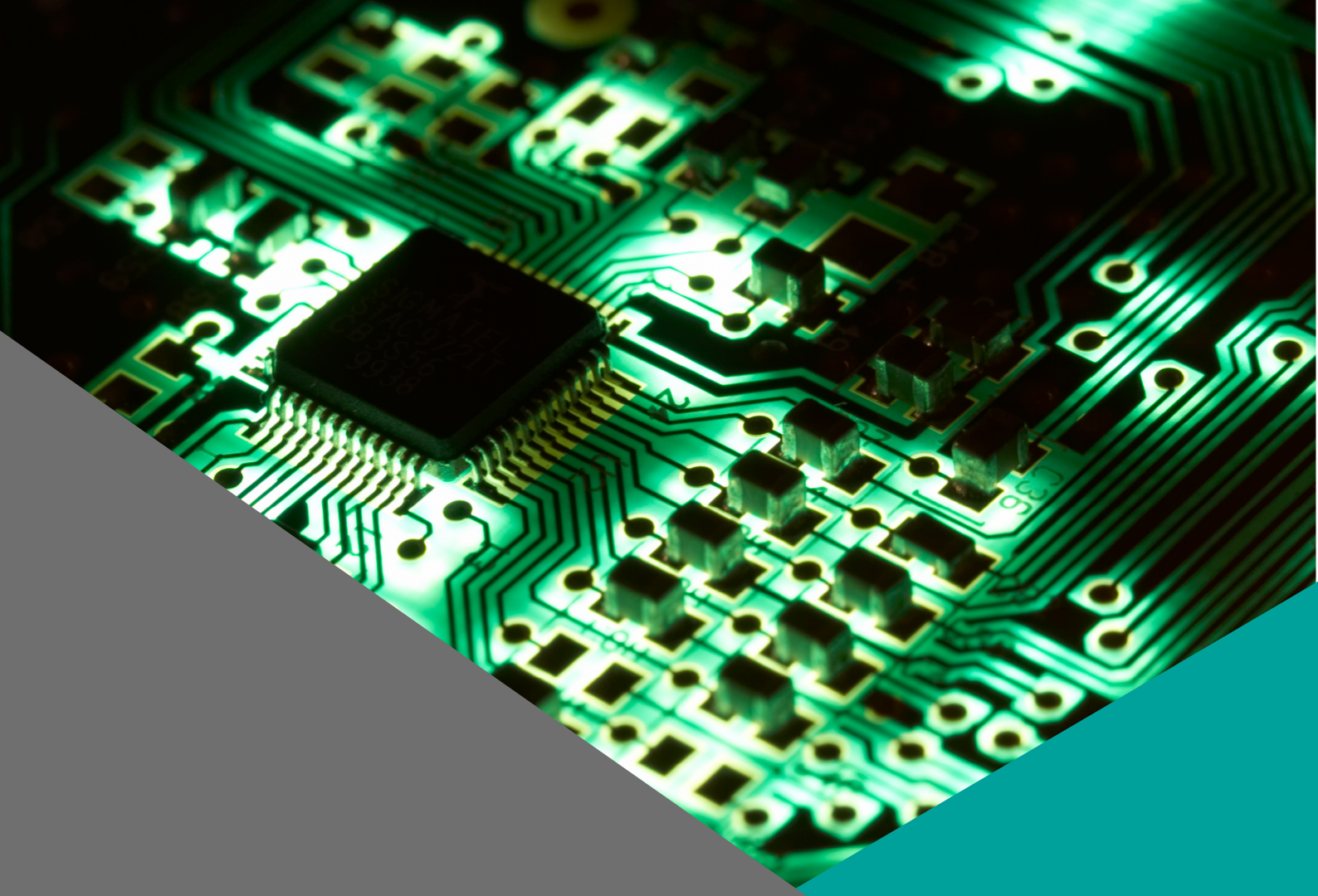

MATERIALS FOR THE
ENERGY TRANSITION

MATERIALS FOR LOW LOSS ELECTRONICS

This publication forms part of the 'Materials for the Energy Transition' series. The Henry Royce Institute in collaboration with the Institute of Physics and the Institute for Manufacturing have convened the academic and industrial materials research communities to explore opportunities for materials to support the UK's net-zero by 2050 target.

HENRY ROYCE INSTITUTE

IOP Institute of Physics

IfM MANAGEMENT TECHNOLOGY POLICY

MATERIALS FOR THE ENERGY TRANSITION ROADMAP:

LOW LOSS ELECTRONICS

SEPTEMBER 2020

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INTRODUCTION

The Challenge: Materials for the Energy Transition

Following release of the Committee on Climate Change (CCC) 2019 Report [1], the UK is committed to a new greenhouse gas emissions target: net-zero emissions by 2050.

The Executive Summary of the **2019 Committee on Climate Change Report** states:

> ***"Delivery must progress with far greater urgency.***
>
> - ***2040 is too late for the phase-out of petrol and diesel cars and vans, and current plans for delivering this are too vague.***
> - ***Over ten years after the Climate Change Act was passed, there is still no serious plan for decarbonising UK heating systems and no large-scale trials have begun for either heat pumps or hydrogen.***
> - ***Carbon capture (usage) and storage, which is crucial to the delivery of zero GHG emissions and strategically important to the UK economy, is yet to get started. While global progress has also been slow, there are now 43 large-scale projects operating or under development around the world, but none in the UK.***
> - ***However, falling costs for key technologies mean that the future will be different from the past: renewable power (e.g. solar, wind) is now as cheap as or cheaper than fossil fuels in most parts of the world."***

In response, the Henry Royce Institute (the Royce), in collaboration with the Institute of Physics (IOP), has engaged with academic and industrial materials research communities to explore solutions to the grand challenge of **"Materials for the Energy Transition"**. Through roadmapping workshops and associated community-led activities, technologies were identified where materials research can make a significant impact on greenhouse gas emissions.

The key drivers for this work have been (1) the pathways to net-zero emissions suggested in the CCC report, and (2) Royce-supported community workshops undertaken in 2019 to identify areas where investment in UK materials science can generate impact and contribute to the UK's energy transition. These included the "Atoms to Devices" workshop in Leeds (May 2019); the "Operando and In Situ Characterisation of Energy Materials" workshop at the Diamond Light Source in Harwell (July 2019); and, the "Multi-Modal Characterisation of Energy Materials" workshop in Cambridge (November 2019).

As a consequence, the following four areas were identified where materials science is critical to enabling a step-change in greenhouse gas reduction:

1. Materials for photovoltaic systems
2. Materials for low-carbon methods of hydrogen generation
3. Materials for decarbonisation of heating and cooling
    I. Thermoelectric energy conversion materials
    II. Caloric energy conversion materials
4. Materials for low loss electronics

[1] Committee on Climate Change Report: Net-Zero, January 2019, https://www.theccc.org.uk/publication/net-zero-the-uks-contribution-to-stopping-global-warming/

Materials Roadmaps

In 2020, the Royce together with the respective research communities explored the various materials challenges, targets, and timescales required to support the achievement of net-zero greenhouse emissions by 2050 of the four research areas outlined above. The CCC report and the related materials community engagement emphasised that these four areas are components of a broader ecosystem of materials technologies which together contribute to the UK's goals to deliver net zero by 2050. These roadmaps form the basis for bringing scientific research communities, industry and government together to address immediate and long-term requirements for the development of a suite of energy materials to replace fossil fuel-based energy technologies. The Royce collaborated with the Institute of Physics (IOP) to set out the programme of work and ensure community-wide feedback and engagement. Skills and expertise from the Institute for Manufacturing (IfM) were commissioned to ensure a robust roadmapping methodology, throughout the series of online roadmapping workshops, and to support community discussions.

Roadmap Objectives and Methodology

The main objectives for the five materials roadmaps at the outset were as follows:

- To understand the current state-of-art for each topic
- To define the most significant technical challenges for each area that are providing barriers to impact on net zero targets
- To define the anticipated future challenges for each area in contributing to net zero targets
- To identify solutions to these challenges that can make step-changes in delivery of technologies to contribute to net zero targets
- To identify the desired performance targets of such solutions

The methodology adopted was based on wide-ranging engagement with research communities to define the roadmap objectives and expectations, to design and customise the strategic framework for the roadmapping, to develop questionnaires for the research communities involved, and to modify workshop process steps to ensure participation of the entire research community. The workshops brought together academic and industrial experts in the four respective technology areas and involved both offline and online data collection phases. The offline phases were used for data collection from individual participants and publicly available research sources, followed by data consolidation and, where necessary and appropriate, prioritisation. The online workshops were used for data review, analysis and deeper exploration of essential issues. The quality and reliability of the process was maintained by a Steering Committee involving roadmapping facilitators and technical leads from each of the four research communities.

In total, 26 workshops sessions were held across the four technology areas between March 2020 and June 2020. These revealed several materials sub-topics of particular interest for contribution towards the net-zero targets, as well as highlighting important fundamental research and commercial technology enablers that need to be established. These outputs significantly aided research communities' understanding of the future direction of energy materials research, towards the achievement UK's net-zero emission targets by 2050.

Between March and June 2020, over 220 participants contributed to the creation of these five roadmaps from the UK academic and industrial materials communities. The outcomes are:

(1) an **executive summary** report, highlighting the main findings of the four roadmapping activities, published in July 2020;

(2) five **materials development roadmaps** towards net-zero emissions for 2050, published for research communities, funding bodies, government, policy-makers and industry leaders.

The five materials roadmaps generated are living documents, and Royce will engage with research communities regularly to review these documents and to develop further roadmaps as new materials systems and technologies emerge. We would like to thank all who have participated in these activities through the roadmapping workshops, interviews, surveys and research summaries.

Oversight of these community activities was through the "Materials for the Energy Transition" Steering Group: Professor Neil Alford, (Imperial College London), Professor Manish Chhowalla (University of Cambridge), Professor Richard Curry (University of Manchester), Professor Edmund Linfield (University of Leeds).

Programme management, reporting, and community engagement was undertaken by Royce and IOP: Mia Belfield (Royce), Ellie Copeland (IOP), Anne Crean (IOP), Isobel Hogg (IOP), Judith Holcroft (Royce), Professor David Knowles (Royce), Dr Amy Nommeots-Nomm (Royce), Dr Suman-Lata Sahonta (Royce), Professor Philip Withers (Royce), Dr Katharina Zeissler (Royce).

Roadmapping activities were coordinated by IfM: Dr Nicky Athanassopoulou, Dr Diana Khripko, Dr Imoh Ilevbare, Dr Arsalan Ghani, Andi Jones, Rob Munro.

Technical oversight of roadmaps was undertaken by Dr Oscar Cespedes (University of Leeds), Dr Katharina Zeissler (University of Leeds), Dr Oliver Fenwick (Queen Mary University of London), Dr Robert Hoye (Imperial College London), Dr Xavier Moya (University of Cambridge), Dr Ifan Stephens (Imperial College London), Dr Sam Stranks (University of Cambridge).

EXECUTIVE SUMMARY

In the context of the UK's ambitious target to bring all greenhouse gas emissions to net-zero by 2050 the development and adoption of more energy-efficient electronic systems are an important enabler for the UK to achieve this goal.

The Henry Royce Institute (UK's national institute for materials research & innovation) supported by the Institute of Physics, brought together over 50 UK academic and industrial experts from different research, fabrication, equipment supply and user fields in a community consultation of nine workshops to explore different materials and methods that are required for the future of such low loss electronics.

The consultation focused on three main areas identified as of the highest impact:

- Materials for Power Electronics
- Materials for CMOS
- Materials for 'beyond CMOS device architectures' ('*More than Moore'*).

Key findings include the needs for:

- Investment to support UK prototyping/pilot-plant scaling of devices from research to wafer-scale fabrication and manufacture, including validation and testing; this provides a supply chain to test and translate new ideas.
- Investment in a network of state-of-the-art 'fab-of-the-future' centres, accessible to the whole UK, encompassing the design, growth and fabrication of new materials. This would be supported by UK Centres in *Materials Replacement & Recycling*, *High-frequency Devices*, and *High-throughput Testing,* each underpinned by world-class scientists and engineers, with dedicated specialist technical staffing
- Development of techniques to effectively and efficiently embed new materials into high performance, energy efficient devices, including interfacing with the external environment.
- Establishment of big data and machine learning (AI) approaches to materials discovery (Materials 4.0) and advancing the understanding of interfacial properties (Interface 4.0), supported by accessible materials databases, and simulation and modelling development across the length scales – from atoms to devices.
- Investment to support the development of new computing architectures, and next generation wide-bandgap semiconductors for power electronics.
- Funding approaches to support UK-wide collaborations between academia and Industry.
- Investments and incentives for industry to undertake research, and lead and develop exploitation strategies.
- Influencing policy, including setting power consumption targets, supporting the circular economy through end of life considerations, and removing reliance on lifecycle supply-constrained materials

It is proposed that these will be critical factors in establishing an environment where the UK takes a leading position and becomes the place for investment for the future development of *low loss electronics*.

Over the next three months these findings will be developed into targeted business cases for funding approaches to support UK-wide collaborations between academia and Industry.

INDUSTRY AND MARKET OPPORTUNITY

Today, an estimated 40% of natural resources are converted to electrical energy. This is expected to grow to 60% by 2040. [2] The way we generate and use electricity will have a huge impact on greenhouse gas emissions. How we use and more importantly how efficient we use electricity to achieve desired outcomes, such as performing a computational task or propelling an electric car will shape our path to net zero and will impact the UK economy. The resulting world market in electronics is worth £602 billion with a predicted growth rate of 2.3% over the next five years. [3] It is also notable that approximately 30% of all electrical energy generated utilises power electronics, with the global market estimated at £135 billion, and a growth rate of 10 % per year. [4] However, in 2019 UK revenue in the electronics sector was reported to be only £1.9 billion, [5] emphasizing the need to stimulate manufacturing and policies in this critically important sector. But this comes at a price. Digital technologies are expected to consume around 21 % by 2030. [6]

To reduce the carbon footprint of digital technologies, improving performance beyond current fundamental limits is critical. But even greater than this is developing new kinds of devices, for all aspects of low loss advanced computing and power conversion. These new devices, which are needed in all things related to Big Data, in IoT, AI, a smart grid, and electric and autonomous vehicles, impact hugely on achieving a green, high quality way of life. The discovery and development of eco-friendly materials lies at the very heart of this area.

[2] ECPE Position Paper Energy Efficiency, https://www.ecpe.org/index.php?eID=dumpFile&t=f&f=3947&token=b101a99377736374bc119ef8da68fd67d99dc545 , (2007)
[3] C. Mieles, IBIS World Industry report C2524-GL Global Semiconductor & Electronic Parts Manufacturing , (2020)
[4] S. B. Reese, et al., Joule 3, 4, 903 (2019), https://doi.org/10.1016/j.joule.2019.01.011
[5] S. Kotze, IBISWorld Industry Report C26.110 Electronic Component Manufacturing in the UK, (2019)
[6] N. Jones, Nature, 561, 163 (2018), doi: 10.1038/d41586-018-06610-y

PROBLEM STATEMENT

The consultation on materials and frameworks for sustainable, low loss electronics is intended to identify ways to enable the UK to meet its goal of net-zero greenhouse gas emissions by 2050. By bringing together academic experts from different materials research fields, the workshops aimed to review the state-of-the-art and set realistic performance targets for materials leading up to the 2050 goal. The workshops fed into a low loss electronics roadmap on sustainable low loss electronics to help the UK to meet its net-zero goal, and is focused on the following high-level questions:

1. Which materials systems and frameworks show the most promise for viable energy-saving applications towards net-zero emissions by 2050, and what is the current state-of-the-art?
2. What are the current materials challenges that limit the deployment of these materials?
3. What performance could be achieved with current materials, and what could be achieved by 2030, and by 2050?
4. What should be the key standards and metrics for the performance of materials and devices?
5. How can improvements be made in the characterisation of these materials?
6. What are the best action plans to integrate a wide range of strategies into highly developed and widely used technologies?
7. How can improvements be made in the provision of advanced facilities required for industry scale-up and commercial testing, in comparison to the availability of suitable lab-scale tools?

Furthermore, a key strategy to enable the manufacturing of materials and devices at commercial scale must be the consideration of **circular economy thinking** and more specifically recycling of materials embedded in devices at the end of life.

The main outputs from the consultation were organised into **research and technology enablers**, **development and scale-up** and **materials** for the energy transition.

The **Materials** identified for the energy transition are:

- **Materials for Power Electronics** – underpinning local energy generation, distribution, and consumer use. This topic focuses on exploiting emergent SiC and GaN technologies; developing next-generation materials (e.g. 3C-SiC, Al(Ga)N, and Ga_2O_3); and, addressing recycling, the scarcity of source materials, and, the whole-life energy costs of manufacture in the electronics sector. Materials include 4H-SiC, 3C-SiC, GaN, Al(Ga)N, Ga_2O_3, BN and B(Al)N, and diamond. Key challenges include fabrication methods and device design and optimisation.

- **Materials for CMOS** – advancing society's digital connectivity and mobility, and supporting the remote operation of ever more complex devices for monitoring of the environment, health and security. This topic focuses on integrating new materials into CMOS devices to demonstrate new concepts (e.g. 'tunnel', 'negative capacitance'), thereby reducing the operating voltage and energy consumption of CMOS. It also considers integration of different materials to enhance significantly device functionality (e.g. delivering compact, low-power, radio-frequency (rf) sources and the incorporation of tuneable materials such as piezoelectrics, antiferromagnetics, plasmonics and photonics, whilst maintaining CMOS compatibility).

- **Materials for 'More than Moore' -** to achieve high computational power with lower energy consumption using new computing architectures, accelerating performance and energy efficiency of computing for the future. This topic addresses the development of new paradigms for computing and information processing. It goes beyond traditional CMOS 'von Neumann' computing (e.g. through developing neuromorphic computing architectures), and is underpinned by new materials, (e.g. spintronic, topological and organic materials), and new device concepts (e.g. chargeless computation and collective switching). Exemplars include (a) nano-oscillatory neural networks; (b) in-memory computing using memristive materials such as redox, phase change, and spin transfer torque materials; ionic synaptic transistors; and, metal-oxide bilayers; (c) edge computing; (d) probabilistic computing; (e) all optical, optoelectronic or magneto-optic computing; (f) quantum computing, with low temperature compatible memory; (g) non-volatile logic operations and (h) chargeless computation utilising spin, the electrical dipole or orbital states in materials such as ferroelectrics, magnetic materials, light metals, semiconductors, 2D materials, organic and molecular materials, topological insulators, quantum wells, molecules and crystals. The key challenges are the identification of the right materials system for the specific targeted computing architecture, and the optimisation of the active materials, and conversion of input/output signals, such as charge current/light to spin current, and vice versa.

Reduction of electronic power consumption and elimination of losses which cause the generation of parasitic heat are key for reducing energy demands of digital processes, and can be achieved through developing advanced functional materials and novel methodologies. **In scope** are the materials developments that reduce heat generation and improve performance of dielectrics, and the design of new frameworks of operation which use spintronics, photonics, metamaterials, negative capacitance, 2D materials, topological insulators, superconducting electronics and neuromorphic computing. Themes **not in scope** are strategies involving quantum computing, communications networks, displays and screen technologies.

The table below summarises the current and anticipated future status of the different materials based on information available in the public domain. The materials outlined within the table are examples and do not represent a comprehensive list.

Category	Sub-Category	Pages	Material	2020-2030	2030-2040	2040-2050+
Power Electronics	Wide Band Gap Materials	16	4H-SiC			
		16	3C-SiC			
		17	GaN			
	Ultra-Wide Band Gap Materials	17	Gallium Oxide (Ga_2O_3)			
		18	Diamond			
		18	Aluminium Nitride			
	Other Novel Materials	18	BN and B(Al)N			
CMOS Integration	Enhancing Current Functionality to Increase Productivity	23	Heterogeneous material integration with CMOS (e.g. Piezoelectrics, ferroelectrics, 2D Materials, III-V semiconductors, antiferromagnets)			
		23	Monolithic integration of different device functionalities (e.g. Si photonics [7])			
	Integration of New Materials into CMOS to Reduce Energy Consumption	25	New Tunnel FET concept development and integration with CMOS (e.g. 2D materials, SOI, Ge, SiO_2, Ta_2O_5, Si-Ta_2O_5)			
		25	Materials for CMOS and negative capacitance (e.g. ferroeletrics doped HfO_2, SiN)			
	Interconnects	27	Cu			
		27	Silicides, carbon based materials			
	Substrate Development for Heat Dissipation	28	Low loss dielectric substrates SiC, GaN, BN			
		28	Low loss dielectric substrates Al_2O_3, MgO, diamond, SiC, high-resistivity Si			
Neuromorphic Computing	CMOS Based	30	Loihi, True North			
	Nano-Oscillator Networks	32	Joule heating oscillators (e.g. $PrMnO_3$)			
		32	Magnetic based oscillators including Spin Torque Oscillators			
		32	Metal-insulator based oscillators (e.g. VO_2, NbO_2)			
		32	Volatile filamentation (e.g. TaO_x)			
Probabilistic Computing	Magnetic	33	Unstable magnetic tunnel junctions			
		33	Interfacial skyrmion materials			
Edge Computing	In Memory Computing	34	Magnetic materials with high perpendicular magnetic anisotropy			
	Sensors	34	Semiconductor sensors, smart sensors, light sensors			
		35	Photoferroelectric materials (e.g. doped and band gap engineered ferroelectric oxides))			
		47	Ferromagnetic and antiferromagnetic materials e.g. as sensor and THz source (e.g. CuMnAs, Mn_2Au, MnN, NiO, Mn(II)Au, CoO, RuO_2)			
Hybrid computing	Optic	37/38	Si photonics			
		37/38	Photonic logic gates			
	Optoelectronic	37/38	Plasmonic and phase change materials (e.g. Ge_2Sb_2Te+InP+Plasmonic nanostructure)			
		37/38	Nanocavities (e.g. InGaAs, InGaAsP)			
	Magneto-Optic	46	Magnetooptically active materials (e.g. GdFeCo, [Co/Pt]/Cu/GdFeCo, YIG:Co,Pt/Co/Gd, Mn_2Au)			
	Continued overleaf…					

[7] D. Thomson, et al., Journal of Optics, 18, 7, (2016), doi:10.1088/2040-8978/18/7/073003

Category	Sub-Category	Pages	Material	2020-2030	2030-2040	2040-2050+
Order Parameter Computing	In Memory Computing	**40**	**Oxides – Resistive materials (e.g. Ta_2O_5, HfO_2, TiO_2)**			
		40	Phase change chalcogenides			
		42	MRAM and Magnetic tunnel junctions (e.g., W/CoFeB/MgO/CoFeB/W/Co/Ru/Co/Pt/Co/Pt]$_6$)			
		41	Ferroelectric (e.g. HfO (doped and undoped), HfO_2-ZrO_2, $PbZr_xTi_{1-x}O_x$, (1-x)[$Pb(Mg_{1/3}Nb_{2/3})O_3$] - x[$PbTiO_3$], $SrBi_2TaO_3$, $BiFeO_3$)			
		41/42	Piezoresistive (e.g. SMS, Heusler compounds, chalcogenides, oxides)			
		47	Antiferromagnetic (e.g. CuMnAs, MnN, NiO, Mn(II)Au, CoO, RuO_2)			
	Spin Current Generation	44	Heavy metals (e.g. Pt, W, Ta, Ir) (e.g. used in memory computing) interfaced with a magnetically ordered material			
		44	Topological oxides (e.g. Bi_2O_3, $SrIrO_3$, $SrTiO_3$, $LaAlO_3$)			
		44	Topological materials and superlattices (e.g. $Bi_{1.5}Sb_{0.5}Te_{1.7}Se_{1.3}$, $Cr_xBi_2Se_3$, Bi_2Se_3, α-Sn)			
		44	2D transition metal dichalcogenides (e.g. MoS_2, MX_2)			
		44	Optically generated spin current (e.g. Bi_2Te_3 on GaAs)			
	Magnetic Manipulation using Magnetoelectric Materials	44/45	Multiferroics (e.g. $BiFeO_3$, $LaBiFeO_3$, $TbMnO_3$, $LuFeO_3/LuFe_2O_4$)			
		44/45	Magnetostrictive (e.g. Fe_3Ga, $Tb_xDy_{1-x}Fe_2$, FeRh)			
		44/45	Exchange Bias (e.g. Cr_2O_3, Fe_2TeO_6)			
	Magnetic Materials	44	Ferromagnetic materials (e.g. Co, Fe, Ni, CoFe, NiFe, CoFeB) (In production in connection with STT MRAM and magnetic information storage, permanent magnets, etc)			
		44	Heusler alloys (e.g. X_2YZ, XYZ: Co_2FeAl, Mn_3Ga)			
		47	Antiferromagnetic materials (e.g. CuMnAs, Mn_2Au, MnN, NiO, Mn(II)Au, IrMn, CoO, RuO_2)			
		49	Nanocarbon and molecular thin films on ultra-thin metal thin films or 2D materials			
		49	Molecular thin film magnets (e.g. Phthalocyanines α-CoPc, carbon based molecules)			
		48	2D van der Waals materials			
	Racetrack and Logic	45	Synthetic antiferromagnetically coupled materials (e.g. TaN/Pt/Co/Ni/Co/Ru/Co/Ni/Co/TaN)			
		45	Ferrimagnetic materials (e.g. AlO/TaN/Pt/Co/Gd/TaN)			
		44	Magnetic logic (e.g. Pt/Co/AlO)			
	Interconnect and Interlayer Materials	46	Metals (e.g. Cu)			
		46	Metals (e.g. Ag, Co, Al)			
		46	Metal semiconductor (e.g. Ru poly-Si, NiSi, CoSi, NiGe, TiSi)			
		46	Interlayer dielectrics (e.g. SiO_2, SiN, SiCOH, polymers)			
		46	Superconducting materials			

Key	Research activity	Industrial prototype	Implemented at industrial scale

Endangered Materials

Many elements in the periodic table feature in electronic devices and technology developments in the low loss electronics space may well impact on this list. Currently there are concerns regarding to the sustainability of our digital lifestyle. The following materials have been highlighted as materials which are under threat of dissipation within the next 100 years. [8] He, Ag, Te, Ga, Ge, Sr, Y, Zn, In, As, Hf and Ta (conflict material). Materials which face a rising threat due to an increased global use are[8]: Cr, Co, Dy, Ru, Rh, Pd, Os, Ir, Pt, U. Materials with limited availability and thus are potentially under risk associated with their supply in the future are[8]: Li, B, Mg, P, Sc, V, Mn, Ni, Cu, Se, Zr, Nb, Mo, Sn (conflict material), Sb, Nd, W (conflict material), Au (conflict material), Ti, Pb and Bi. Conflict materials are materials that are often mined in mines where wars are fought over their ownership.

As new materials systems and products are developed scarcity, accessibility, ethical and responsible sourcing, and end of lifetime recycling are important considerations to ensure a sustainable digital society. Recovery of materials from electronics devices at the end of their lifecycle is a vital part of a sustainable circular economy. Research efforts are needed to develop high performing materials to tackle our dependency on endangered materials which cannot sufficiently be recovered. **The main recommendations** for developing low loss electronics include:

- Investment to support UK prototyping/pilot-plant scaling of devices from research to wafer-scale fabrication and manufacture, including validation and testing; this provides a supply chain to test and translate new ideas.
- Investment in a network of state-of-the-art 'fab-of-the-future' centres, accessible to the whole UK, encompassing the design, growth and fabrication of new materials. This would be supported by UK Centres in *Materials Replacement & Recycling*, *High-frequency Devices*, and *High-throughput Testing,* each underpinned by world-class scientists and engineers, with dedicated specialist technical staffing
- Development of techniques to effectively and efficiently embed new materials into high performance, energy efficient devices, including interfacing with the external environment.
- Establishment of big data and machine learning (AI) approaches to materials discovery (Materials 4.0) and advancing the understanding of interfacial properties (Interface 4.0), supported by accessible materials databases, and simulation and modelling development across the length scales – from atoms to devices.
- Investment to support the development of new computing architectures, and next generation wide-bandgap semiconductors for power electronics.
- Funding approaches to support UK-wide collaborations between academia and Industry.
- Investments and incentives for industry to undertake research, and lead and develop exploitation strategies.
- Influencing policy, including setting power consumption targets, supporting the circular economy through end of life considerations, and removing reliance on reliance on lifecycle supply-constrained materials

It was recognised that any material and technology development in this area needs a **sustainable** and stable resource supply as well as **end of life recycling** options to enable the sustainable, long-term use of these technologies.

[8] D. Cole-Hamilton, Periodic Table: new version warns of elements that are endangered, (2019), https://theconversation.com/periodic-table-new-version-warns-of-elements-that-are-endangered-110377

For **research and technology enablers**, the requirements include:

- Materials Discovery and Development, supported by artificial intelligence (AI) and machine learning approaches, measurement and analysis, and understanding of the characteristics and dynamics of materials and their interfaces.
- Simulation and Modelling, including ab-initio atomistic and empirical/phenomenological models to determine fundamental material parameters, underpin electronic and opto-electronic device designs, and interpret and predict experiment.
- Benchmarking testing protocols and databases to compare with existing technologies and devices, including use of high-throughput testing, and scale-validated proxies, with new testing standards enabling translation from development laboratories to large scale pilot lines.
- Recyclability and recovery of materials, including identifying incentives, targets and life-cycle analysis when selecting materials and processing routes, and considering availability of scarce materials and the whole-life energy cost of manufacture and use.
- Partnerships to stimulate the exchange of ideas between academia, industry and research institutions (both within the UK and outside). This should include provision of incentives for industry to co-develop fundamental research programmes from the outset, and embedding of Universities into a lab-to-product research and development culture

For **development and scale-up**, the requirements include:

- Pilot line facilities to move device concepts from academia to industry accompanied by suitable industrial certification and demonstrations of scalability, thereby establishing an ecosystem and supply chain. Exemplars include integration of new materials with CMOS, large-scale integration of III-V semiconductors with silicon, and scale-up of wide bandgap semiconductors and silicon photonics to wafer fab.
- Development of the manufacturing technologies required for new materials integration, alongside and complementary to established techniques, including deposition (e.g. MBE, PLD, CVD, ALD, PVD), processing, patterning, annealing, and validation of quality, uniformity, and functionality.
- Centrally-managed facilities (e.g. Research Training Organisation) to support scale-up, fabrication, component development, testing, seeding of commercialisation, and incentivising and support of start-ups, with specialist staff, consolidated and dedicated equipment, and on-going funding for proving projects, and training of manufacturing and technical staff.
- Enabling Technologies and Skills to accelerate product development by understanding design processes and process control in 4th Industrial Revolution (4IR) manufacturing processes.
- Routes to market, provided through engagement with early adopters from industry, as well as engaging with multi-national end users and global foundries, and supporting the commercialisation of intellectual property arising from the UK research base.

MATERIALS FOR POWER ELECTRONICS

BACKGROUND

Power electronics is the key technology to control and convert the flow of electrical energy from the source to load-side consumption. Applications include consumer products, electricity generation from wind and solar energy and electrical vehicles. Currently, the energy losses from power electronics are high and savings of more than 50% could be achieved[2] with the development and use of low loss power semiconductor devices. [9] For example, advanced power electronics could reduce the electrical energy consumed by motor drives by 20-30% in the developed world[2]. Advanced materials for power electronics can contribute towards these targets.

The current, most widely used material in power electronics is silicon. Advanced fabrication processes and sophisticated electronic device designs have optimized the silicon electronic device performance almost to their theoretical limit. [10] To further improve the performance of power electronic devices new materials need to be developed that can operate at higher voltages, faster switching speed, and at higher temperature. Not only will this lead to more efficient power conversion solutions, but these will also be lighter and smaller, with less cooling requirements.

THE STATE-OF-THE-ART AND CURRENT CHALLENGES

The current, most widely-used material in power electronics is silicon (Si). Si-based power electronic devices have some critical limitations, such as[9]:

- *High losses* due to the low critical electric field (25 V/µm) of Si that leads to unipolar devices (MOSFETs, Schottky diodes) with high resistance and therefore high conduction losses.
- *Low Switching Frequency* due to the need for bipolar devices (IGBTs, thyristors) in order to keep conduction losses low.

Material research activities [11] have been focusing on improved switches, for example having higher blocking voltage, on-state current density, and switching frequency. Many developments are also taken place on the device level with integration of logic and power circuits in a single chip, reliability improvements, thermal management and packaging.

MATERIAL DEVELOPMENTS

The crucial materials' property for high performing power electronics devices is a high critical electric field. Materials with a critical electric field higher than Si enable power electronic devices to withstand higher voltages for a given drift region width. Alternatively, they can be exploited to produce much more efficient devices at a given voltage, with reduced losses and faster switching, the result of the drift region having been scaled down. Other important factors include a wide bandgap which enables high temperature operation, and a high thermal conductivity which improves the dissipation of heat, reducing operational temperatures. This improvement in the thermal management reduces external heat sink requirements and lowers cost. A high charge carrier saturation velocity also helps increase switching frequencies.

[9] ARPA-E Power Electronics Paper, https://arpa-e.energy.gov/sites/default/files/documents/files/ARPA-E_Power_Electronics_Paper-April2018.pdf , (2018)
[10] P. J. Wellmann, ZAAC, 643, 21, (2017), DOI: 10.1002/zaac.201700270
[11] 'Power semiconductors – state-of-the-art and future trends', Vitezslav Benda, Czech Technical University in Prague, Transaction on Machine, Power electronics and Drives ISSN: 2229-8711 Online Publication, (2011)

New material developments in this domain have been focussed on developing and testing wide band gap (WBG) semiconductors, SiC and GaN, and ultra-wide band gap (UWGB) semiconductors, diamond, Gallium Oxide and Aluminium Nitride (as well as more novel materials such as Boron Nitride (BN). Developments on silicon [12] are taking place at the device level, in the form of integration of logic and power circuits on a single chip and in form of improvements on the reliability and thermal management and packaging.

Wide Band Gap Materials

SiC and GaN address the performance shortcomings of Si, however, their non-negligible defect densities and high synthesis costs are limiting factors for large scale applications. [13]

SiC is, of all "beyond Si" contenders, the most technologically mature materials system. 4H-SiC unipolar devices (MOSFETs, Schottky diodes) of high quality and increasing maturity and reliability, are available from a number of international suppliers in the voltage range of 600 to 3300 V. Drivers of device development are the electric vehicle and solar inverter markets. However, a number of materials issues are preventing the production of devices at other voltages. Bipolar devices, potentially rated up to 30 kV per device, are not currently possible due to the number of defects in the substrate, and in the epitaxy, which reduces the carrier lifetime. Furthermore, all substrates are highly n-type doped, the absence of p-type substrates, making it a significant processing challenge to make n-channel IGBTs. Finally, high voltage devices require thick epitaxially grown drift regions, which is currently prohibitively expensive due to slow growth rates and hence throughput. The UK is taking the lead in resolving many of these issues, [14] addressing improvements in epitaxial growth processes and device design and development.

A large number of different stacking sequences of the Si-C double layer exist resulting in various stable crystal polytypes which exhibit differences in their electronic properties, including their band gap and charge carrier mobility. 4H-SiC is the polytype that is in production, as detailed above. 3C-SiC, which must be grown upon another substrate such as silicon, is attractive due to its potential compatibility with existing silicon lines. However, its material quality is currently poor, the number of defects very high due to its growth on a different substrate. With capability in the UK to grow both polytypes, and to fabricate high voltage devices, a significant opportunity exists to strengthen its position in this growing market.

GaN devices are being manufactured internationally however, the technology maturity is slightly behind SiC.[15] GaN possesses excellent characteristics when compared with silicon with a high breakdown capability, high blocking voltage using thinner devices, higher electron mobility than silicon and silicon carbide, and higher critical field resulting in a thinner more highly doped drift layer and thus lower on-resistances. In combination this results in reduced system size and weight and an increased efficiency. It has a higher bandgap than silicon (3x) and SiC (1.1x) and a critical electric field strength 11 times larger than Si. Ongoing materials development towards achieving the theoretical limit of the materials is ongoing as well as improving doping capabilities. In particular, dopant control (principally p-type) for GaN requires more development. This is an important area of research to enable the development of high performance vertical devices with effective termination structures, [15] a type of device structure which is important for reducing switching losses and therefore essential for more energy efficient performance as they can support higher current densities within a smaller footprint. The current focus of materials development is on controlling the

[12] High Power electronics, https://www.sciencedirect.com/topics/materials-science/high-power-electronics
[13] P. Gorai, et al., Energy Environ Sci, 12, 3338, (2019), https://doi.org/10.1039/C9EE01529A
[14] EPSRC Centre for Power Electronics, http://www.powerelectronics.ac.uk/
[15] Y. Shi, et al., Sci. Rep.,9, 8796, (2019) 10.1038/s41598-019-45177-0

number of defects in GaN which is limiting the size of size at which wafers can be grown. Issues with bowing and thermal effects on large GaN on Si wafers limits the effective wafer size, an aspect needing further development. Furthermore, development is directed towards optimising the UK capability in regrowth of GaN on GaN substrates to enable very thick (~100 µm) active layers in devices. Overall, the GaN material now needs to bridge the gap from a laboratory-based material and device development towards volume production within the UK.

Required Activities	Implementation timescale *
Scale-up of GaN materials for device applications	ST
Scale-up of 4H-SiC materials for high voltage device applications	ST
Development of efficient thermal management, including heterogeneous integration	ST
Dopant control (principally p-type) for 3C-SiC, and GaN	ST-MT
Solve issues with Issues with bowing and thermal effects on large GaN on Si wafers	ST-MT
Materials for device application beyond Si (2-300V), 300-900V GaN, >SiC for Automotive applications	MT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

Ultra-Wide Band Gap Materials

Ga_2O_3 offers the potential for high voltage operation and low cost wafer production. [16], [17] [18] Gate-to-drain electric field strength of >3.8 MV/cm have been shown in beta-Ga_2O_3 metal oxide semiconductor field effect transistors, a value which exceeds theoretical limits for GaN and SiC, while still affording scope for improvements. [19] Currently, Ga_2O_3 devices have an issue with heat dissipation that can be addressed by using diamond as a heat sink. Development of efficient thermal management methods which can be integrated into the growth process are critical for device development. Further research into p- and n-type doping capabilities is needed. Currently p-type doping in Ga_2O_3 is quite problematic as doped materials tend to display low mobility. Furthermore, limits exist in the capability of high background n-type doping as Ga_2O_3 needs a high concentration of acceptor dopants. Modelling and simulation is an important aspect of research for both improving the Ga_2O_3 material performance as well as enabling device design development. Solutions that link in with device processing and packaging methods are needed also.

For **diamond**, doping remains a key research area. A breakthrough in doping is fundamental for diamond to fulfil its ultrahigh bandgap potential. Future research activities need to demonstrate relevant diamond transistor architectures. However, developing the materials growth capabilities of diamond is also of interest for other power electronics devices due to its thermal properties and thus its potential to act as a heat sink.

The development **AlN** and **AlGaN** materials for power electronic devices is still in the early stages. Applications are envisaged in the medium-term (2025-2035) potentially for 12kV and high frequency operation. The research challenges are focused on high quality growth of these materials and specialist facilities are needed for growing these high mole fraction materials. Issues with regards to how to achieve the required doping need to be addressed.

[16] J. Yang, et al., IEEE Electron Device Letters, 38, 7, (2017), DOI: 10.1109/LED.2017.2703609
[17] Z. Hu, et al., IEEE Electron Device Letters, 39, 6, (2018), DOI: 10.1109/LED.2018.2830184
[18] S. B. Reese, et al., Joule, 3, 899, (2019), https://doi.org/10.1016/j.joule.2019.01.011
[19] A.J. Green, et al., IEEE Electron Device Letters, 37, 7 (2016), https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7470552

Other Materials

Further research is required for **BN** and **B(Al)N**, and the applications could be realised in the long-term (2035+). It is not clear presently if the performance of these materials would superior to the other UWBG ones discussed in this and previous sections. However, large scale computational screening has identified nine **oxides**, four **nitrides** and three **carbides** as possible candidates for future research efforts (e.g. zinc oxide could be a material of interest for high temperature and high power applications [20]). A screening of 863 materials, taking into account heat dissipation as a performance factor[13], has shown that there is scope for fundamental research for power electronics research of the future.

Required Activities	Implementation timescale *
Development of BN and other promising candidates for future device applications	LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

Device Developments

For all power electronic devices research is required on the materials used for device processing, e.g. dielectrics, contacts, ultra-conformal high-K dielectrics, soft magnetic materials for power inductors and transformers, die-attach, interconnect, encapsulation materials for power packaging, thermal interface materials for cooling, and feedstock materials for additive manufacturing for heterogeneous integration. [21] This is essential in order to develop reliable devices. There is a high innovation potential in research on novel insulators.

Required Activities	Implementation timescale *
Ability to control rapidly changing magnetic fields	ST-MT
Passive components development like high-frequency inductors	MT
Smart power IC, where the logic device sits alongside the power substrate).	MT
Systems to deliver integrated working devices	MT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

UK CAPABILITY

The EPSRC Centre for Power Electronics[14] has strongly supported the development of SiC material, devices and applications in the UK, unifying research efforts from across academia and industry. Work within this Centre has helped to pioneer a range of high voltage SiC power devices, including the epitaxy and the device development. Within the UK, epitaxial growth of SiC is available from the University of Warwick [22] and Clas-SiC [23] in Scotland, with volume production taking place at the IQE plant in Newport. [24] SiC device development capability exists at the Universities of Warwick and Newcastle, and in Clas-SiC, while device design expertise exists in the Universities of Cambridge and Nottingham. Ion implantation capabilities are available at the University of Surrey. [25] There are no suppliers of SiC substrates in the UK.

[20] M. Benlamri, et al., ACS Appl. Electron Matter, 1, 1, 13, (2019), https://doi.org/10.1021/acsaelm.8b00053
[21] A Special Edition for Advanced Power electronics, ISSN 1996-1944 (2019) https://www.mdpi.com/journal/materials/special_issues/materials_power_electronics

[22] https://warwick.ac.uk/fac/sci/eng/research/grouplist/electricalpower/peater/sicepitaxy
[23] https://www.clas-sic.com
[24] https://www.iqep.com/about-iqe/
[25] https://www.ion-beam-services.com/

The UK has a strong footing in GaN growth capacity within academia (for example at the Universities of Sheffield, [26] Cambridge[26] and Nottingham [27]). Foundry capability exists at IQE and with some III-V on Si capability at Newport Wafer Fab for up to 200 mm wafers. Swansea hosts Ga_2O_3 MOCVD growth facilities which is an excellent first step in developing a UK capability. No dedicated reactors are available, however, within the UK for novel materials beyond Ga_2O_3 and hence materials produced tend to suffer from inferior quality. This has resulted in outsourcing of AlN and AlGaN wafer growth. In general, a review of epitaxy facilities within the UK is needed. Capabilities need to be updated to keep up with international competition if the UK wants to stay relevant in the power electronics sector.

Whilst the UK is very strong in compound semiconductor technologies and bringing these through TRLs 1-3, the transition into the higher value TRLs for the applications markets is behind this. It is vital that the infrastructure is put in place to avoid a cyclic opportunity cost on UK technologies being developed and then exploited overseas. Indeed, substantial investments are being made in Europe, America and Asia in order to attain dominance in the development of next generation low loss electronics markets, and it is imperative that the UK is in a position to compete internationally.

[26] Metalorganic Chemical Vapour Deposition (MOCVD)
[27] Molecular Beam Epitaxy (MBE)

UK COMMUNITY RECOMMENDATIONS

There is an enormous market opportunity for **SiC** devices, especially for automotive applications, but in order for the UK to compete internationally, investments are needed. The community recommends investments into new and existing SiC facilities in industry and academia. A further **two epitaxial growth facilities** (up to 6" wafer size) in academic institutions would help tackle the fundamental issues that remain in the growth of the material. Further investments into existing and new **SiC fabrication facilities, with >6" wafer size capability** would enable translation of research into the commercial space. This will allow the UK research and industrial communities to continue to compete internationally and take a lead in this rapidly expanding field. In particular, SiC fabrication capabilities need specialist equipment, such as **high-temperature furnaces for annealing and oxidation, and PECVD systems**, along with the capability any Si fabrication facility will require. More **GaN** regrowth capability is needed within the UK, including 'fast' epitaxy to enable the formation of ultrawide (~100 µm) layers. There is also a need for an expansion and enhancement of f**abrication capabilities expansions,** such as access to state-of-the-art gate recess capability (digital etch). In addition to growth and fabrication facilities this needs to be accompanied by state-of-the-art **standards and reliability testing** facilities.

For developing both **SiC** and **GaN** devices not only significant capital investments required, but also continuous and consistent funding for fabrication-related projects, and to develop the UK's skills and to establish a highly trained workforce. It is important that the UK can demonstrate a sovereign capability in this strategically-important area, as well as continuing to undertake international co-development, especially with European partners post-Brexit. Enhanced doping capabilities are needed, especially p-type doping, on the national level such as pulsed epitaxy for dopant control. Co-location of epitaxial growth and fabrication centres is essential for ensuring that material and device developments progress to higher TRL levels (e.g. prototyping and manufacture). For early TRL developments, a virtual centre would enhance the UK effort. A dedicated facility supported by characterisation experts for a wide range of characterisation methods such as DLTS, Hall, CV, fast-transient analysis is needed to enable material parameter (mobilities, phonon modes, lifetime etc.) extraction and thus support new device design. There are significant limitations in translation of academic knowhow into an industrial setting with limited access to testing facilities. A UK pilot line facility is needed to enable new materials developments to be tested in an industrial manufacturing setting without contaminating existing fabrication lines. These investments are essential to provide rapid, efficient access of the whole UK community to state-of-the-art tools and to allow the UK to compete internationally.

Future development is needed of **Ga_2O_3**, together with expanding capabilities for halide vapor phase epitaxy (HVPE), and low-cost polycrystalline materials growth. Demonstration of working Ga_2O_3 devices is needed by 2025 in order to remain competitive with the international developments in this rapidly-growing field. There is also a need for fundamental discovery-led research into future wide band gap materials for power electronics and high temperature operation, taking into consideration the abundance of source materials, the need for recycling, and the importance of sustainability over the full materials life cycle.

MATERIALS FOR CMOS

BACKGROUND

Complementary metal–oxide–semiconductor (CMOS), is a well-established semiconductor fabrication process that is used for constructing both digital integrated circuits e.g. microprocessors, memory chips and analogue ones such as RF circuits and sensors. CMOS and related technologies are vital for designing high performance, low power devices. [28]

The semiconductor manufacturing industry particularly those related to small scale electronics are scaling down devices continuously. Due to the dramatic reduction in device size, numerous challenges are surfacing related to energy consumption, heating, connectivity and integration of new materials. To overcome these challenges disruptive innovation in materials and devices is required, in two broad areas (a) increasing the device functionality or productivity without increasing the power consumption and (b) reducing the energy consumption in the next three decades. Substrate development is also essential for heat dissipation.

However, there are many issues into integrating novel materials with CMOS processing, such as differing processing temperatures, achieving stable interconnections between the different materials or avoiding contamination. Development of CMOS compatible deposition techniques (e.g. ALD) which enable scalable control of material composition and thickness at the atomic level are key towards accelerating the transition between laboratory based research and product manufacturing.

THE STATE-OF-THE-ART AND CURRENT CHALLENGES

CMOS for high-performance electronics is right at the theoretical limit. Most industrial drive is focused in reducing transistor size to improve performance per square inch. Challenges need to be addressed in order to reduce the power consumption by 90%, by 2050, and minimise the cooling requirements while retaining comparable length scales without compromise to performance i.e. speed.

Enhancing the current device functionality: Due to the high barrier to enter the market, new low power technology ideally possess the following features: (i) they are “drop-in” replacement for CMOS FETs; (ii) they are compatible with CMOS processes; and (iii) they significantly improve performance, reduce cost, or add novel functionality beyond the current capability of CMOS. In order for an ‘enhanced CMOS technology’ to be adopted, there is an absolute requirement that the replacement significantly outperforms its existing CMOS alternative.

Despite the scaling and energy challenges of CMOS and the quest for “beyond CMOS” technologies, the industry continues to innovate and invest in CMOS based devices. This is highlighted by planned multi-billion dollar investment in silicon fabrication facilities in 2020 and beyond. Thus, there is significant barrier for adoption of any new technology. Ideally, any new technology must be CMOS compatible and offer new functionalities that enhance the current CMOS capabilities.

Materials challenges for CMOS integration include the following:

1. Interface engineering to optimise metal/semiconductor junctions and reduce contact resistances.

[28] T. Chen, 2006 8th International Conference on Solid-State and Integrated Circuit Technology Proceedings, (2006), DOI: 10.1109/ICSICT.2006.306040

2. Interconnects need to be optimised There is an urgent need to develop low dielectric constant (k < 2) materials. High k dielectrics are not available for most new semiconductors which is an issue not only at the device level but also at the system level. The absence of low k materials leads to large resistance-capacitance power dissipation. This is where a lot of thermal impedances and thermal mismatch occurs due the difference in the thermal coefficient of expansion of materials. This is a problem which spans from the micro-level through to the system level.
3. Ability to downscale to the nano-scale.
4. Ability to move from 2D to 3D.
5. Etching and processability of different materials and their compatibility with CMOS processing.
6. Operating temperature range between different materials.

With regards to the **reduction in energy consumption** per switching for low-voltage devices, the signal-to-noise ratio is a key limitation. Reduction of the device operating voltage requires improvements in signal-to-noise ratio to allow efficient power utilisation and optimisation. A reduction of parasitic losses such as heat generation via Joule heating, through negative capacitance for example, is necessary.

MATERIALS FOR ENHANCING CURRENT FUNCTIONALITY

The limitation of traditional CMOS technology is the struggle to improve performance, reduce power consumption and increase bit density while maintaining or reducing wafer cost. To go beyond traditional CMOS we need to add functionality to CMOS while in parallel reduce the energy consumption. For the future, the focus is on high mobility, low leakage materials to improve performance without increasing power consumption. A summary of the performance of different materials beyond Si in terms of carrier mobility and energy bandgaps can be found in reference. [29] Furthermore, key advances can be made by adding materials which can be actively tuned to enhance functionality for example by adding ferroelectrics, plasmonic or magnetic materials. Growth of heterogeneous materials on large-area silicon platforms (8”-12”) to enable large scale manufacturing is a challenge.

Heterogeneous Material Integration with CMOS

Heterogenous material integration with CMOS has taken place for over a decade for example by using silicon-germanium (SiGe).

Silicon Carbide (SiC) integrated with CMOS has been demonstrated already in both digital and analogue circuits extending the operating temperature up to 500 °C [30] which is not possible with Si alone. SiC is also of interest for CMOS integrated RF applications. The SiC growth capabilities are discussed in the power electronics section of this report.

Piezoelectric materials can be integrated into transistor gate stacks to improve MOSFET behaviour as well as add sensing capabilities. Using nitrogen-polar AlN as part of the gate stack allows for example the detection of different magnitudes of force applied to the device. This opens the doors to applications ranging from varying sensor systems, niche RF applications, actuation and to energy harvesting. [31] Dielectric materials which enable this technology are Si_3N_4, AlN, ZrO_2, HfO_2 or $HfSiO_4$. While large area and large volume growth

[29] High mobility materials for CMOS applications, Chapter 2: Opportunities and challenges of multiscale heterogenous material integration on Si platforms for enhanced functionality and performance, Aaron V.-Y Tean, NUS, Singapore. ISBN 978-0-08-102062-3, (2018)
[30] C. Zetterling, et al., Semiconductor Science and Technology, 32, 3, (2017) https://iopscience.iop.org/article/10.1088/1361-6641/aa59a7/pdf
[31] H. Winterfeld, et al., Journal of Material Science: Materials in Electronics, 30, 11493, (2019), https://doi.org/10.1007/s10854-019-01502-x

and fabrication capability is available these are not suitable to trial and develop niche applications, where intermediate-scale facilities are needed.

The development of **2D** and **thin film** materials compatibility with Si is an active research activity. Graphene has promise in terms of performance however interfacing graphene with other materials such as electrodes is a challenge. High quality CVD grown graphene can be used as a plasmonic material adding further functionality. Proof of concept for its use for optical switching/signal processing has been demonstrated and could be manufactured within the next 5 years. The main challenges lie in dry transfer or low temperature deposition methods on top of CMOS without contamination. Graphene can be grown in-situ on Si and alternative substrates (SiC, BN saphire and GaN) without the need of dry transfer has been demonstrated by the companies such as EMBERION and PARAGRAF. Early proof-of-principle on a single device scale are in the public domain for graphene and ferroelectrics however, a proof of scalability is still outstanding.

GaN is an important material for future RF microwave devices for high frequency communication. Of particular interest here is the integration of efficient RF communication with CMOS on the same chip. In particular, in the area of **5G operation and beyond**. The 5G materials demands are substantial and the UK research in materials for 3G and 4G has been central to defining new modalities – this must continue with 5G. The challenge is achieving sub-100 mV switching at 50 GHz operation enabling agile antennas (beyond 5G). In the longer term 6G (>50 GHz) development will push all technologies and materials.

Monolithic Integration of Different Device Functionalities

Silicon waveguides on thick layers of silica, integrated onto silicon are important for a range of applications. This includes silicon photonics, inertial sensing and quantum technologies.
Research activity focused on interfaces is required. Interfaces need to demonstrate low loss dielectric properties. Multiple research and development capabilities are required spanning physics, modelling, structure-functionality relationships and final device performance prediction.

Required Activities	Implementation timescale *
Fast materials evaluation and testing capability including in operando testing and device testing on the die. Testing needs to fit with existing processes, and needs to be coupled with site-specific off-line quality assurance, as well as on-line monitoring.	ST
Model performance of RF switch.	ST
Big data intelligence, 4th Industrial Revolution strategy for manufacturing to accelerate product development.	ST
Scoping of scenarios for developing power consumptions for policy. RE, PR, scalability is known, DE loss, RF switch.	ST
Modelling (including ab Initio modelling) of the system is needed that includes structure-functionality relationships and final device performance prediction capacity by intelligent behavioural design.	ST-MT
Understand the device scaling behaviour more generally	ST-MT
Fundamental physics research on fermi levels, bandgaps, etc. is needed	ST-LT
Understand the effect of defects on material and device performance	ST-LT
Research on interfaces that need to show low loss dielectric properties. Multiple research and development capabilities required (physics, modelling, structure-functionality relationships and final device performance prediction.)	ST-LT

Research and development of new 2D materials to perform different functions beyond plasmonics	MT-LT
Development of high quality, new piezoresistive composites materials. Using the state-of-the-art, they are only just good enough versus other systems.	MT-LT
Optimisation of metallic conductors and development of new oxide conductors	MT-LT
Pilot capability for niche applications and demonstration of scale-up, e.g. piezoelectrics on silicon and silicon waveguides. This needs to be accompanied with suitable certification to match industry requirements (which is normally available in Universities)	ST-LT
Improvement of 12" high quality Piezoceramic materials growth for RF switch applications and development of UK manufacturing capability	ST-MT
Improvement to yield and performance of piezoelectric devices	ST-MT
"Tools" (MBE, PLD, CVD, ALD, PVD) development for new materials systems for quality, uniformity, functionality. Tool manufacturers are keen to do this but are not UK based. This will also have to address the adaptation of the in Laboratory-to-Fab toolsets	MT-LT
Make up-to-date equipment for monolithic integration to be available to academic researchers, such as pick-and-place, wafer-, and on-chip bonding (to demonstrate integration capabilities).	MT-LT
End-users need to be brought in	MT-LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

INTEGRATION OF NEW MATERIALS INTO CMOS TO REDUCE ENERGY CONSUMPTION

Power consumption in CMOS is typically due to charging and discharging of capacitors (dynamic power consumption), short circuit paths and leakages from diodes and transistors. As devices scale down, static power dissipation when devices are on stand-by mode also become significant. The challenge is developing and implementing technologies which reduces the power consumption of current technology by at least a factor of 100 while retaining comparable length scales and performance.

To reduce power consumption of CMOS devices per switching requires optimisation at all levels i.e. the technology used to implement the digital circuits, as well as the circuit design and architecture. The primary strategy for reducing power consumption is reducing and controlling the threshold voltage. For this the signal-to-noise ratio is a key limitation.

There are four possible ways: (i) energy filtering in tunnel FETs, (ii) inter voltage amplification using negative capacitance gates, (iii) metal insulator transitions using phase change materials (i.e. colocation of memory and computing which is covered in more detail in the beyond CMOS materials section of this document), and (iv) internal transduction such as spin FETs.

Tunnel field-effect transistor development and integration with CMOS

Tunnel field-effect transistors (TFETs) enable the device to be switched off more effectively that a more conventional transistor. For example, TFET logic consumes only 54% of total CMOS power. [32] A number of TFET designs depend on heterojunctions of different materials such as GaSb/InAs. [33,32] Interfaces play a critical role in device optimisation for power efficiency as a poorly controlled interface tends to induce leakage currents through high level of traps and defects. [34] Development of homo-junctions where only one junction material is used and optimisation of the doping levels could help solve this issue. TFETs also face scale-down challenges. The need to fabricate very thin body dimensions to achieve good electrostatics and the requirement for high quality III-V materials and their oxides to remove the effects of trap-assisted tunnelling are challenges. The former could be addressed by using atomically thin 2D semiconductors. 2D semiconductors are ideally suited for TFETs and provide unique CMOS compatible process advantages. 8" compatibility is important for any technology development. Here the focus needs to be on medium scale innovation.

Negative capacitance materials

Negative capacitance is an important strategy for reducing energy consumption which could be integratable into a CMOS stack. Negative capacitance circuits are analogue building blocks that can be used to compensate for undesired parasitic capacitance, bandwidth enhancement of amplifiers, equalization filters design without passive inductors, etc. [35, 36] Negative capacitance materials are simple ferroelectric materials and their feasibility has been demonstrated. However, it is challenging to achieve non-hysteretic negative capacitance FET using ferroelectric materials. Further research needs to be focused on compatibility and integration with CMOS using low-temperature deposition methods for as well as on improving the yield and performance of those materials.

[32] U. E. Avci, et al., Journal of the Electron Devices Society, 3, 3, (2015), https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7006647
[33] U. E. Avci, et al., (2013), IEEE International Electron Devices Meeting, DOI: 10.1109/IEDM.2013.6724559
[34] K. Derbyshire, TFETs And/Or MOSFETs For Low-Power Design, (2017), https://semiengineering.com/tfets-andor-mosfets-for-low-power-design/
[35] https://ieeexplore.ieee.org/document/6240619
[36] https://doi.org/10.1038/s41598-019-45628-8

There is no manufacturing of negative capacitance materials in the UK currently. Manufacturing facilities exist in Finland (DCA [37]) and the Netherlands (Solmates [38]). It is important to create an ecosystem and establish an upstream industry e.g. chemical manufacturing. To address this knowledge gap, it is important to develop a clear understanding of which applications could benefit the most from these materials. Deposition capabilities of high-quality films on 12" wafers need to be developed. Negative capacitance ferroelectric layers should be CMOS compatible and need to be trialled initially to develop capability in the UK to stimulate industrial uptake. Of particular interest here is the development of materials growth capability using CMOS fabrication compatible tools such as ALD.

Research is required in both fundamental material understanding and development as well as manufacturing process capability and equipment. A list of the different research activities proposed is shown in the table below.

Required Activities	Implementation timescale *
Develop controlled etching capability	ST
Develop and improve testing equipment for Traps	ST
Validate testing method and develop new testing standards for various material systems	ST
Eliminate hysteresis for negative capacitance materials	ST-MT
Matching of negative to positive capacitor to achieve steep switching and improve understanding for device design	ST-MT
Non-native dielectric knowledge could be leveraged to understand trap distribution time-constant and space-location. Progression of native to non-native dielectrics. Getting control of dielectrics, profound understanding of various dielectrics rather than silicon e.g. Gallium Nitride. Maintain activity on all Nitride based structures e.g. Gallium Nitride.	ST-MT
Develop understanding what is going on in process chamber relating to deposition, particularly understanding dimensions like flow rate, pressure, energy control, charge, chemical composition, material properties and using big data simulations to get meaningful results to control process.	ST-MT
Understanding and controlling material properties for device performance and in particular research in doping and contacts especially to wide-bandgap materials	ST-MT
Understanding process variables and linking to product performance especially in CMOS.	ST-LT
Understand process dimensions and process control using Big-Data Analytics for control strategy in manufacturing processes.	ST-LT
Improve ability to generate 2D Hole gasses	ST-LT
Use Density function theory for modelling and simulation and T-CAD models for a range of materials	MT-LT
Develop a common platform - Gap in ALD and ALE, Select Area Deposition infrastructure	MT-LT
Develop equipment and technologies to understand process chambers relating to deposition. Furthermore, equipment and processes to capture flow rates, pressure, energy control, charge, chemical composition and material properties and then applying appropriate big data analytics to get meaningful results for robust process control to get appropriate product performance	MT-LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

[37] https://www.dca.fi
[38] https://www.solmates.nl

INTERCONNECTS

Interconnects are a critical research area that needs to be developed in parallel with other material developments for integration with CMOS. Currently Cu is used as interconnect material, but it exhibits issues such as increased scattering at the surface and grain-boundary interfaces when it is scaled down. [39]

Development of new, low k dielectrics and highly conducting materials is necessary to overcome the limitations of Cu. New conductors have been investigated such as silicides and materials that have different conductance mechanism e.g., carbon.

Silicides have low resistance, good process compatibility with Si, make good contact with other materials and show little electromigration. **Carbon-based materials** such as multiwalled Carbon Nano-Tubes (CNT), mixed CNT bundles and multilayer graphene nanoribbons (GNR) are emerging as promising materials for interconnects. [40]

Additional materials' development to use for Cu barriers is also required to prevent Cu diffusion e.g. Ta(N), Mn(N) etc. or materials to improve the adhesion properties of low-k materials[39].

SUBSTRATE DEVELOPMENT FOR HEAT DISSIPATION

The development of future low loss electronic devices, including (a) the integration of new device functionalities with CMOS, (b) the enhancement of power electronic performance, and (c) the development of new computing architectures, are all underpinned by the development of suitable substrates. High thermal conductivity materials are needed in which the thermal expansion of the substrate is matched to that of the active layers, and with high interfacial adhesion to integrated metal surfaces or other films. The substrates need to be large area, and have low defects, low bow, and be robust to thermal cycling. They also need to have low electrical loss.

Low loss dielectric substrates

High resistivity Si is well established and commonly used, especially in optoelectronic integrated circuits. Additional research is needed for large wafer diameters and for RF applications. p-type Si is currently used for GaN growth for power electronics.

Silicon Carbide (SiC) substrates are becoming widely used in power electronic devices, as well in other applications such as the development of photovoltaic cells. They are also being used as the host substrates in low loss applications of GaN-based materials. However, due to the strong Si–C covalent bands, it is hard to fabricate high density SiC substrates at low processing temperatures without the use of additives or external pressure. [41]

GaN has several advantages for use in optoelectronic and high power and high frequency electronic devices. The issues are the lattice mismatch between GaN and conventional substrates such as sapphire, silicon or silicon carbide resulting in poor crystal quality and hence high dislocation density, pits and cracks that affect carrier transport. Therefore, there is a strong need to develop bulk free-standing GaN substrates. [42, 43] There have been successful methods to grow bulk GaN. However, there are still issues with large scale thick

[39] The International Roadmap for devices and systems: 2017, IEEE, (2018)
[40] S. M. Turkane, et al., International Journal of Electronics, 104, 7, (2017), https://doi.org/10.1080/00207217.2017.1285436
[41] G. Magnami, et al., Journal of the European Ceramic Society, 34, 15, 4095, (2014), doi: 10.1016/j.jeurceramsoc.2014.06.006.
[42] H. M. Foronda, et al., Journal of Applied Physics, 120, 3, (2016), https://doi.org/10.1063/1.4959073
[43] H. Amano, et al., Journal of Physics D: Applied Physics, 51, 16, (2018), https://iopscience.iop.org/article/10.1088/1361-6463/aaaf9d

GaN growth due to wafer bow. Additional issues exist around the scalability of the fabrication methods and cost. Polycrystalline **AlN** needs developing for growth of GaN (CTE matched substrate) for power electronics.

Development of **Ga_2O_3**, and substrate technologies is required to overcome the limitations in existing materials. Development activities need to include growth, contacting, processing and testing.

Diamond has excellent thermal properties and therefore the potential to act as a heat sink. This particularly important for power electronic devices and diamond is considered as a substrate for RF electronics applications. Diamond is also used for optical sensing/single photon applications. There are several material issues to overcome for the fabrication and use of diamond substrates such as ability to fabricate large size substrates that are dislocation free, and of low resistivity. [44] Diamond is required to be doped to make it useful for the design of devices, which has been difficult to achieve.

Sapphire (Al_2O_3) and **MgO** single crystals can both be made in large areas and both have good thermal conductivities and low microwave dielectric loss.

Required Activities	Implementation timescale *
Addressing limitations of the Laboratory-to-Fab toolsets, which need to be adapted	ST
Analysis and testing that fit with processes, and with the need for site-specific off-line quality assurance, as well as on-line monitoring.	ST
Pilot capability to take SiC and GaN from University facilities to wafer fabrication. Deposition is needed, but also suitable processing, patterning, and annealing.	ST-MT
Modernising testing and analysis equipment for high power applications. There are opportunities for manufacturers to develop new test equipment for RF and power applications.	ST-MT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

[44] S. Shikata, Diamond and Related Materials, 65, 168 (2016), https://doi.org/10.1016/j.diamond.2016.03.013

UK COMMUNITY RECOMMENDATIONS

The materials challenges identified are mainly around the translation pathway from academia to manufacturing. Having 8" compatibility is important, but the focus should not be on foundries but on providing innovation on the medium scale. III-V on silicon for lasers needs to be scaled from academia to industry, with buffers needed for scale up to 12" wafers. The UK has an 8" CMOS line, and 4" and 6" experimental lines. It is of importance to establish equivalent modelling and simulation methods to obtain good yields as well as detailed simulations of all aspects of the fabrication process. As more, and different, materials are envisaged for incorporation with CMOS, it will be critical to consider cross-contamination issues. As materials are scaled up from research, interface and defect control will become critical. Materials will need development and optimisation, and growth methods/toolsets will need to be adapted accordingly. This requires dedicated materials research scientists.

In order to advance niche applications, a short-term focus on developing patterning and structuring with the aid of a foundry service is needed for small scale production (1000 die per annum). Integration of new materials such as piezoelectrics on silicon for sensing, niche RF applications and actuation (MEMs, and IoT) to demonstrate feasibility are important. Large area and large volume capability is available, however this is not suitable for niche applications, where cost effective intermediate-scale facilities are needed. Such a foundry would need to support a disparate materials set while avoiding potential contamination.

There is a recognition that excellent research is being undertaken by UK scientists and engineers in academia, but the UK lack the Institutes and Centres seen in Europe, the US and far-East (e.g. IMEC, the Fraunhofers, Chalmers, TNO and the National Labs in the US) to take new materials and devices from TRL3 to TRL7. Such Centres embed a culture of translation of ideas to commercialisation, and have industry embedded within them. The advantages of such a National Institute are retaining expertise in materials and devices through core groups of long-term scientists, engineers and technicians. The UK provides outstanding training for people in materials science and engineering however, retention of these talents within the UK is currently challenging. Institutes, separated from individual University, help retain talent and serve as links to other international Institutes and Centres. DARPA for example has funded a $1.5B *Electronics Resurgence Initiative*, illustrating the importance of electronic materials and their commercialisation.

There is a need to support start-ups in accessing equipment and specialist staff especially as devices become more complex and involve many materials and interfaces.

UK expertise is focused on the know-how of complex materials and technologies for the future. These need to be tested and proved, ready for scale-up from research. Simulation and modelling feedback is needed for studying interfaces, defects, and reliability analysis is becoming more and more crucial.

MATERIALS FOR MORE THAN MOORE

The long-term goal is to realistically power computationally intensive, by current standards, tasks through green energy such as solar and wind. For a step change in the energy efficiency of computing there is a need to move away from ferrying electrical signals around electronic chips in series. Progress in advanced signal multiplexing and a continuing development in co-locating memory and processing is essential. New hardware solutions need to be found and implemented to support the fast evolving software developments. New building blocks need to be conceived and improved, not restricted to CMOS technology, which deliver on improved performance and energy efficiency.

Required activities	Implementation timescale
Electrical applications powered autonomously	**MT**
Boosting silicon capabilities	**MT**
Fully autonomous remote applications which are self-powered and utilise local energy harvesting	**LT**
Achieve conventional computing at a fraction of the current energy consumption.	**LT**
Unsupervised learning integrated into a dynamic environment such as controlling interfaces for autonomous vehicles.	**LT**
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

NEUROMORPHIC COMPUTING

Neuromorphic computing refers to computing which emulates the neural structure of the human brain. This is especially suitable for develop computing hardware and software which tackle data intensive problems however which do not require high accuracy, i.e. task which the human brain excels at such as image recognition. Existing computing and logic architectures are extremely good at deterministic problems but are very inefficient and power intensive at solving indeterminate problems e.g. image recognition. One way of realising neuromorphic computing is via artificial spiking neural networks. In a spiking neural network neurons fire independently but are linked and thus a fired neuron changes the electrical state of connecting neurons. This leads to information being encoded in the signal itself but also in their timing and thus learning occurs by a dynamical remapping of the synapses in response to stimuli.

Intel's most recent Loihi chip includes 8,000,000 neurons optimised for spiking neural networks performing tasks with 10,000 times energy efficiency at 1000x faster performance when used for applications like sparse coding, graph search and constraint-satisfaction problems (Intel's neuromorphic Loihi processor scales to 8M neurons, 64 cores [45]). Beyond von Neumann computing solutions developed by IBM and brought to market contains 256 million 'neurons' per system, *True North* architecture e-brain chips project. Both platforms are still largely based on CMOS transistors the former on 14nm CMOS technology and the latter on 40 nm CMOS technology. [46]

[45] J. Hrjuska, Intel's Neuromorphic Loihi Processor Scales To 8m Neurons, 64 Cores (2019), https://www.extremetech.com/computing/295043-intels-neuromorphic-loihi-processor-scales-to-8m-neurons-64-cores

[46] B. Linares-Barranco, et al., Nature electronics, 1, 100, (2018), https://doi.org/10.1038/s41928-018-0028-x

Neuromorphic computing and artificial intelligence go hand in hand. The first generation of AI developed by Intel was rule based and emulated classical logic in order to draw reasoned conclusions in a very specific and well-defined problem domain, thus performing tasks more energy efficiently. Efforts of the second generation of neuromorphic computing are focused on sensing and perception. Thus, target areas are deep-learning networks and the analysis of a video frame. The next generation, as Intel sees it, will extend artificial intelligence towards mimicking human cognition. The focus will be on interpretation and autonomous adaptation, addressing the lack of context and common-sense understanding present in the second-generation artificial intelligence chips. In order to achieve this, a key factor is the development of neuromorphic computing and probabilistic computing tool boxes. The latter creates algorithmic approaches to dealing with uncertainty, ambiguity and contradiction in the natural world. In summary, neuromorphic computing enables unsupervised learning and probabilistic computing will enable a computer to cope with the chaos of the natural world. Combined artificial chips will move towards matching a human's flexibility, and ability to learn from unstructured stimuli with the energy efficiency of the human brain, estimated at 20 W.[46]

Required activities	Implementation timescale*
Research into new material platforms with designed properties for non von-Neumann computing.	ST
Improvements on CMOS based artificial intelligence based technology	ST
Improvements on supervised learning	ST
Demonstration of supervised hardware learning.	MT
Development of non-CMOS based technology including non CMOS neurons	MT
Development of Bio-inspired 3D architectures	MT
Achieve unsupervised learning and artificial intelligence which mimics human cognition with a focus on interpretation and autonomous adaptation which demonstrates common sense and understanding of context	LT
Implementation of non-CMOS based neural networks	LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

Nano Oscillator Networks

Taking inspiration form the brain's neurons which behave like non-linear oscillators which develop rhythmic activities and interact to process information, artificial networks of coupled oscillators have great potential for high density, low power neuromorphic computing [47]. The key challenge to high-density, low-power neuromorphic computing is the realisation of large networks (initially 2D to be expanded into 3D long term) of oscillators in the order of 10^8 devices which fit on a reasonable sized chip. In other words, each oscillator needs to possess a lateral dimension which is less than 1µm and does not suffer from noise and stability issues[49]. CMOS oscillatory networks are under investigation, such as ring oscillators and Schmitt trigger-based oscillators however challenges with frequency tunability, complex circuit design involving 10-20 transistors and high-power densities persist. [48, 49] Laboratory based prototypes of non-CMOS alternatives are emerging. Under consideration are Joule heating, $PrMnO_3$, [50] volatile filamentation, TaO_x (not area scalable),[50, 51] metal to insulator transition VO_2 and NbO_2 [52, 53] and magnetic switching-based oscillators. [54] Classification of 512 visual patterns into a set classes using a network of 3x3 thermally coupled vanadium dioxide oscillators and one output neuron [55] (Joule Heating oscillators basic operation criteria's have been demonstrated using coupling elements which include a capacitor and a resistor [50]).

Spintronic oscillators are nanoscale pillars composed of composed of magnetic layers separated by a non-magnetic spacers. An applied input charge current is converted into a spin current exerts a torque on the magnetisation of the ferromagnetic layers and generates sustained precession of the pillar's magnetisation. The frequency of the precession has an intrinsic memory with regards to past inputs (of the order of a few hundred nanoseconds) and is sensitive to, i.e. is influenced by the oscillation of neighbouring oscillators.[54] The latter aspect of magnetic oscillators is a key advantage as the nano-oscillator precession is modulated by radio waves however, importantly active oscillators also emit radio waves and thus oscillators in the network interact with each other without the need to implement physical interconnects. This enables wireless communication between oscillators i.e. between neuron layers on the chip. [56] Vowel recognition using coupled nano – oscillators was demonstrated by using 4 coupled nano-oscillators achieving a recognition rate of 85 % using an automatic real time learning rule. This was achieved by tuning their frequency via two strip lines situated above the network. [54]

[47] J. Torrejon, et al., Nature, 547, 428, (2017), https://doi.org/10.1038/nature23011
[48] F.C. Hoppensteadt, et al., IEEE Trans Neural Netw, 11, 3, 734, (2000), DOI: 10.1109/72.846744
[49] S. Lashkare, et al., IEEE 39, 9 (2018), DOI: 10.1109/LED.2018.2854732
[50] A.A. Sharma, et al., IEEE J. Explor. Solid-State Comput. Devices Circuits, 1, 58, (2015), https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=7140766
[51] T.C. Jackson, et al., IEEE J. Emerg. Se. Topics Circuits Syst, 5, 2, 230 (2015), 10.1109/JETCAS.2015.2433551
[52] N. Shukla, et al., Sci. Rep., 4, 4964, (2014), https://doi.org/10.1038/srep04964
[53] Y. Zhou, et al., IEEE Electron Device Lett., 34, 2, 220, (2013), DOI: 10.1109/LED.2012.2229457
[54] M. Romera, et al., Nature, 563, 230, (2018), https://doi.org/10.1038/s41586-018-0632-y
[55] A. Velichko, et al., Electronics, 8, 1, 75, (2019), https://doi.org/10.3390/electronics8010075
[56] A. Slavin, et al., IEEE IEEE Transactions on Magnetics, 45, 4, 1875 (2009), DOI: 10.1109/TMAG.2008.2009935

Required activities	Implementation timescale*
Exploration of new materials which consider the whole ecosystem of neurons and synapses	ST
Development of improved oscillator coupling and synchronisation	ST
Solve challenges associated with size, agility and reproducibility	ST
Achievement of increased efficiency in generating oscillation	ST
Identification of materials which are cost-effective	ST
Improvement of grown materials quality i.e. reduction of defects	ST
Improvement in interface control	ST
In case of magnetic oscillators the following materials properties need optimisation: efficient generation of spin currents, voltage control of anisotropies, more efficient spin torques and efficient manipulation of spin current polarisation	ST
Engagement between academia and industry to establish the future potential of oscillator networks	ST
Development of modelling tools which span length scales from the atomic scale, device scale through to the integrated scale to improve hardware design	MT
Development of proof of principle chip for industry	MT
Identifying and solving manufacturing and scale up issues	MT
Continue the exploration of new materials, considering the whole ecosystem of neurons and synapses	MT
Integration of prototype with computational hardware	LT
Development of hardware connects and software to utilise oscillator chip	LT
Demonstration of large-scale manufacturability and scale up	LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

The main **bottle neck** is that there are no pilot plant for translation of proof of principle to prototype.

PROBABILISTIC COMPUTING

Probabilistic computing hardware and software addresses the challenge of handling the uncertainty and noise which is inherent in data generated from real world events. Modern computing needs to be able to handle and understand uncertainties in order to respond to dynamic environments. This is of importance in autonomous systems where the system needs to be able to understand uncertainties in sensory input in order to make appropriate decisions. High level brain function emulating neural network models which are capable of reasoning and memory recall, often require the presence of noise [57]. However, probabilistic computing is not only a building block for artificial intelligence but can also aid in handling errors in current semiconductor chips.

[57] J. Jordan, et al. Scientific Reports, 9, 18303, (2019), https://doi.org/10.1038/s41598-019-54137-7

Software developments are steadily moving forward. Intel accelerated its investment into modelling the potential impact of probabilistic computing on artificial intelligence in 2018. [58] Materials for probabilistic computing are predominantly in the proof of principle and thus academic domain. Hardware implementations of probabilistic computing use a robust classical entity which fluctuates in time between well-defined 0 and 1 states. [59] A proof of principle device consisting of an asynchronous probabilistic computer based on engineered unstable magnetoresistive random-access memory units (CoFeB/MgO/CoFeB based structure) was achieved.[59] An alternative approach is demonstrated through thermal diffusion of topological magnetic quasi particle entities referred to as skyrmions. [60]

Required activities	Implementation timescale*
Exploration of proof of concept materials and devices.	ST
Design of new hardware aligned to software developments.	ST
Design and materials optimisation	MT
System integration	MT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

The main **bottle neck** is the development of hardware and fusion with software.

EDGE COMPUTING AND AUTONOMOUS SMART SENSORS

Edge computing refers to performing data analysis closer to the point of its creation, i.e. close to the sensor Conventional vision, audio and electromagnetic sensors generate large volumes of redundant data. Transmitting raw data from thousands of sensors to a central processing unit is bandwidth limited and can be costly. An alternative is to bring the computation closer to is generation i.e. performing computation locally and transmit relevant data reducing cost and improving latency issues. [61, 62] Efficiency is at the heart of edge computing and it is a necessity for the internet of things. Furthermore, utilising neuromorphic sensors which produce spiked outcomes in an asynchronous and event-based manner will further reduce data volume. Ultimately edge computing provides faster more relevant and more reliable experiences and helps uncovers business opportunities by tapping into a fast amount of unanalysed and underused data.[64]

"By year-end 2023, more than 50% of large enterprises will deploy at least six edge computing use cases deployed for IoT or immersive experiences, versus less than 1% in 2019". [63] In particular, applications which rely on fast responses and which require ultralow latencies (below 1 ms) will rely more and more on edge computing such as autonomous vehicles, augmented and virtual reality and, industrial robots. [64]

Types of edge computing include the combination of light sensing electronics with a neural network on the same chip. This approach allows the photosensitivity of the light-sensing diodes to be adjusted externally which enables the filtering of useful information at the point of creation and reduces the demand on the computational image recognition algorithm. This is particular useful for driverless cars and industrial

[58] M. Mayberry, Probabilistic computing takes artificial intelligence to the next step, (2018) https://newsroom.intel.com/editorials/probabilistic-computing-takes-artificial-intelligence-next-step/#gs.8iwgq6
[59] W.A. Borders, et al., Nature, 573, 390, (2019), https://doi.org/10.1038/s41586-019-1557-9
[60] J. Zazvorka, et al., Nature Nanotechnology, 14, 658, (2019), https://doi.org/10.1038/s41565-019-0436-8
[61] IBM, What is edge computing, https://www.ibm.com/uk-en/cloud/what-is-edge-computing , (2020)
[62] M. Satyanarayanan, et al. Nature Electronics, 2, 42, (2019), https://doi.org/10.1038/s41928-018-0194-x
[63] Exploring the Edge: 12 Frontiers of Edge Computing, Gartner T. Bittman, Distinguished VP Analyst - Exploring the Edge: 12 Frontiers of Edge Computing, Gartner Research
[64] K. Kitayama, et al. APL Photonics, 4, 9, 090901, (2019), https://doi.org/10.1063/1.5108912

robots. [65] Commercial products are being launched. Sony announced the release of the world's first image sensor with integrated AI earlier this year, its IMX500 sensor which integrates processing power and memory enabling machine learning-powered computer vision tasks. [66]

The core principle of edge computing and autonomous ('smart') sensors is the ability to distribute computational workloads across a sea of low-power devices to achieve improved performance. To achieve this, efficient allocation of tasks across a combination of general and specialist processors is required. Currently this translates into large area requirements and power consumption. Short-term, this can be mitigated considerably by developing more efficient programmable control architectures for heterogeneous systems**.** The control architecture can account for up to 70% of the area, 80% of the latency, and 60% of the power consumption. Modifications using existing technology have already shown improvements of 8%, 22%, 16% in area, latency and power respectively. [67] Currently, silicon-based field programmable gate arrays (FPGAs) and embedded memory application-specific integrated circuits (ASICs) are leading components for the development of edge computing. However, the control architecture and the movement of data around the system is continuing to limit their usage in extremely low-power devices. Further improvements will rely on the availability of integratable non-volatile memory options.

Key considerations in decentralised edge computing and autonomous sensors are durability and reliability as regular repairs and upgrades are not desirable. As such materials research is needed to develop durable, economically feasible embedded memory platforms with scaled down feature sizes. A combinatory approach to materials discovery and optimisation between AI driven modelling, taking into account semi-empirical performance metrics, and systematic materials studies is needed to search the large materials space for suitable hardware candidates. Novel memory platforms will play a key role in the development of edge devices. In particular, the development of low-cost, high-bandwidth, and high-endurance non-volatile memory, which will remove most of the standby power used by the devices. Improvement strategies involving switching to SRAM-based FPGAs to decrease the power overhead is challenged by the significant increase in delays encountered at low-voltage operation which is not feasible for real-time IoT devices. The comparatively short lifetime and slow access times of flash/solid-state memory makes it problematic for the use in edge devices. Magnetoresistive Random Access Memory (MRAM) currently shows the most promise for long-term development of flexible memory technology (in-memory computing, control architectures, and standalone memory) due to its high-endurance. However, a scaling down of device size is needed in order to reach gigabyte-scale in standalone and embedded memory. Furthermore, the device and system must be tolerant to faults within the device which develop over time as the memory is continuously rewritten and the processor is reconfigured.

A critical device design consideration is the battery lifetime in particular for remote sensor operations. There are two main approaches to tackling this problem: 1) to design the device in such a way that the battery will outlast the lifetime of the device or 2) to include energy harvesting materials which collect enough energy to sustain device operation. One class of materials which are of interest for sensor and energy harvest application include photoferroelectric material [68] such as doped ferroelectric oxides e.g. Bi_2FeCrO_6, $(K_{0.5}Na_{0.5})NbO_3$-$Ba(Ni_{0.5}Nb_{0.5})O_{3-\delta}$ (KNBNNO). [69] Photoferroelectric materials are photovoltaic, ferroelectric, piezoelectric and pyroelectric and thus can harvest or sense light, thermal and mechanical energy. Furthermore, they can be grown using CMOS compatible techniques (such as PLD) and promise efficiency on small scale. Laboratory based proof of concept of a working device has been demonstrated. [70] Challenges lie in the materials optimisation in order to improve their photovoltaic, pyroelectric and piezoelectric properties.

[65] W. D. Heaven MIT technology review, (2020), https://www.technologyreview.com/2020/03/04/916701/ai-chip-low-power-image-recognition-nanoseconds
[66] Sony's first AI image sensor will make cameras everywhere smarter, (2020), https://www.theverge.com/2020/5/14/21258403/sony-image-sensor-integrated-ai-chip-imx500-specs-price
[67] X. Tang, et al., Design, Automation & Test in Europe Conference & Exhibition (DATE), (2020), doi:10.23919/DATE48585.2020.9116478
[68] Y. Bai, Adv. Mater. 30, 34, 1707271, (2018), https://doi.org/10.1002/adma.201707271
[69] Y. Bai Adv. Mater. 29, 29, 1700767 (2017), https://doi.org/10.1002/adma.201700767
70 Y. Bai et al. Energy Technology, 2000461 (2020)

Required activities	Implementation timescale*
Addressing niche connectivity, information and security challenges	ST
Development of self-powered units (link to PV and thermoelectric strand)	ST
Set up of closed-loop development programme including constant contact between academics, industry, foundries as well as end customers to inform the materials development	ST
Development of semi-empirical material performance metrics to aid in AI-assisted material discovery	ST
Design and fabrication of heterogeneous control architectures using Si-based SRAM	ST
AI-assisted exploration of platinum-group secondary and ternary alloys for high-endurance, scalable, non-volatile memory (known to have high PMA, compatible with CMOS and high durability)	ST
Band gap engineering of photoferroelectric materials in parallel to finding morphotropic phase boundary regions	ST
Undertake business feasibility study of photoferroelectric materials to support fundamental revolution of design of current sensors and its relevant systems towards multifunctional energy harvesting and autonomous sensor systems	ST-MT
Transition from use of actives sensors which rely on constant energy supply and shift towards passive sensors which harvest their own energy from their surroundings	MT
Improvement of photoferroelectric materials properties especially optimisation of the photovoltaic, ferroelectric, piezoelectric and pyroelectric properties.	MT
Address integration challenges of photoferroelectric materials with CMOS technology (e.g. growing ceramics and single crystals at low temperature (<120° C)	MT
Proof of principle of large scale manufacturability of photoferroelectric materials	MT
Matching hardware to the software algorithm	MT
Application specific neuromorphic sensor development	MT
Autonomous fault detection and offloading of computational work to connected devices to prevent downtime	MT
Exploration of possibility to move toward more than 2-bit readout to increase density	MT
Development of CMOS compatible materials growth of durable materials	MT
Development of reproducible and uniform fabrication techniques as feature sizes decreases to increase densities.	MT-LT
Development of a standard testing platform to address individual or clusters of memory/processing elements in large and potentially reconfigurable arrays of different underlying materials.	MT-LT
Production of Gigabyte-scale standalone non-volatile memory within foundries	MT
Specialised integration of high-endurance non-volatile memory into low-power and compact commercial devices	MT
Possibly a material interface connection to test back end of the line compatibly of a large set of materials	
Widespread distribution of technology through integration into off-the-shelf devices	LT
High-sensitivity and high-speed write and readout mechanisms need to be developed due to much lower voltages involved in the process to distinguish different states	MT-LT

Development and incorporation of energy harvesting materials such as photoferroelectric materials into edge computing device	LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

ALL OPTICAL AND OPTOELECTRICAL COMPUTING

Using light as medium for data transport through intensity modulation for example has the advantage of operating at the speed of light. Translating the advances made in the communications field, where encoding information as optical signals is the norm, onto on-chip optical computing requires devices which work seamlessly in the electrical and optical domain without the need for repeated electrical-to optical conversion. Nanophotonics is an energy efficient and fast way of processing data on a chip overcoming the shortcomings of electric circuits in terms of signal transportation and resistance-capacitance delays which are increasingly problematic as bit rates increase. [71] However, integration of optical and electronic architectures is challenging due to the fundamentally different interaction volumes of electrons and photons. [72] Crucial developments needed are integrated light sources, photodetectors and modulators. Combining elements concepts from the fields of photonics, electronics and plasmonics limitations can be overcome.

While integrated hybrid chips using light and electronics components in combination utilising their respective advantages for improved performance are not realised yet advances in new materials, our understanding of light at the nanoscale and increasing integration density of devices are indicators towards achieving all optical or hybrid computing. Laboratory proof of principle devices towards optical and optical and electrical hybrid functionalities exist. [73], [74], [75], [76], [77], [78] One such example uses a combination of waveguide-integrated plasmonic nanogaps with phase change memristive cells ($Ge_2Sb_2Te_5$) to create an electro- optical memory cell with a switching energy of 16 pJ and an active area of 0.05x0.05 μm^2.[73] Similar outcomes can also be achieved by replacing the phase change material by magneto-optical materials. Another example uses InGAs, and a InP photonic-crystal platform with an imbedded InGaAsP nanocavity to demonstrate the first experimental proof of optoelectronic integration at only 2 fF with data rates of 40Gbit/s and an energy consumption of 42 42 aJ bit^{-1} [73](Advances in silicon photonics is another avenue to achieve optic based computing in the long run as it builds upon fabrication capabilities developed for CMOS [79]).

[71] K.Nozaki, et al., Nature Photonics, 13, 454, (2019), https://doi.org/10.1038/s41566-019-0397-3
[72] Within sight of computing at the speed of light, (2019), https://www.technologynetworks.com/informatics/news/within-sight-of-computing-at-the-speed-of-light-327869
[73] Farmakidis, et al., Science Advances 5, 11, (2019), DOI: 10.1126/sciadv.aaw2687
[74] P. Markov, et al., ACS Photonics 2, 8, 1175 (2015), https://doi.org/10.1021/acsphotonics.5b00244
[75] A. Joushaghani, et al., Opt. Express, 23, 3657, (2015), https://doi.org/10.1364/OE.23.003657
[76] Y. Lu, et al., Nano Letters, 17, 150, (2017), https://doi.org/10.1021/acs.nanolett.6b03688
[77] M. Rude, et al., ACS Photonics 2, 6, 669 (2015), https://doi.org/10.1021/acsphotonics.5b00050
[78] C. Rios, et al., Nat Photonics 9, 725, (2015), https://doi.org/10.1038/nphoton.2015.182
[79] A comprehensive outlook is given on power efficient optical communication technology in the "Roadmap on silicon photonics" D. Thomson et al Journal of Optics, 18, 7 (2016) and in "The health of photonics" an Institute of Physics report (2018). All optical logic includes concepts of cavity-based all optical flip-flops and logic gates, all optical gates based on semiconductor optical amplifiers and nanoscale all-optical logics which are summarised in the following road map (P. Minzioni, et al., Roadmap on all-optical processing, J. Opt. 21, 063001, (2019).

Required activities	Implementation timescale*
Improvement of electron to photon and photon to electron conversion	ST
Communication between industry and academia outlining integration challenges	ST
Improving fatigue issues of hybrid systems	ST
In case of all photonic systems address limits in the power efficiency of silicon based light sources	ST
Reduction of Si waveguide losses to below 2dB/cm	ST
Power efficient on chip integration of lasers through low loss interfaces between III-V and silicon on insulator waveguides within laser cavities	ST
Heat flow management for III-V materials	ST
Small size, large bandwidth, power efficient optical electrical optical converters	ST
Utilisation of AI to accelerate materials discover	ST
Initiate dialogue with photonics community to accelerate hybrid schemes	ST
Investigation of new multifunctional materials ongoing to the long term e.g. 2D materials (large scale manufacturing needs to be addressed in parallel) and heterostructures	ST
Development of reconfigurable system in form of active reconfiguration through 'Etch-o-sketch' type systems, plasmonic particles.	MT
Overcoming miniaturisation challenges concerning operation.	MT
Addressing of integration challenges	MT
Development of advanced hybrid systems converting information from spin to photon. Addressing of issues of gain and amplification (into long term)	MT
Development and implementation of proof of concepts of 3D optical integration	MT
Overcome technological problems with multiplexing. Optimisation of jitter noise instead of amplitude noise levels	MT
Demonstration of chip integration of long distance optical connects	MT
Solve electronic transduction challenge by improving interfaces between electronics and photonics/optoelectronics	LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

MATERIALS ORDER PARAMETER COMPUTING

The goal here is to move away from charge current driven devices and move towards for example spin currents. This has the potential to lead to dissipation less information transport, eliminating Joule heating losses. These thermal effects limit current CMOS technology and preventing devices to operate below around 0.5 V. [80] For this computing, interconnects and memory needs to be redesigned to rely on order parameters such as polarisation, magnetisation, antiferromagnetic order, strain and exhibit collective switching where the target volume switches its order parameter collectively when the input driving signal exceeds a threshold. Furthermore, the output is required to be interconnectable to further logic devices. The transferred output signal then is needs to be able to act as an input signal i.e. achieve a switching event. The last piece of the puzzle is reversibility i.e. once the state is toggled further input from the circuit can reverse

[80] S. Manipatruni, et al., Nature, 565, 7737, 35, (2019), DOI: 10.1038/s41586-018-0770-2

the order parameter back to its initial state. Of interest here are ferromagnetic, ferroelectric or ferroelastic materials.

The building blocks for achieving new logic devices beyond CMOS are devices which outperform CMOS and offer further multi-generational scalability. Key considerations are operation voltage, interconnects and energy consumption[80]. Fundamentally, the challenges in order parameter devices for computing are efficient order parameter switching and effective order parameter detection additionally to the challenge of the interconnects. A comprehensive review of desired parameters operation at 420 K is given in reference [87] and summarises to the following: an element size of 10 x10 nm^2 operating at switching energies of 1-10 aJ, switching voltages of 100-300 mV, switching speeds of 10-1000 ps, write errors of 10^{-1} for stochastic computing and 10^{-12} for von Neuman computing applications. Coupled with electrical and spin current interconnects of 30 nm width and 100nm to 0.1 mm length and switching voltages and currents of 100 mV and 1-10 µA, in case of optical connects 200 nm width and >100um range with a spin to optical conversion at < 10 aJ (10^{-18}J) per bit, 1 Gbit s^{-1}.

In Memory Computing

Resistive memory devices, referred to as memristors, are a relative mature concept, with much research having been done in the last >10 years. Resistive switching materials enable the merging of information processing with memory, and thus reducing the level of electrical signal retrieval and sending from the central processing unit to the external memory across the computing chip. This greatly increases energy efficiency. This class of materials includes transition metal oxides (resistive materials), phase change materials, magnetic multilayer systems and other systems (e.g. ferroelectrics). Potential applications include non von Neumann computer architectures with reduced energy consumption and increases processing speeds. These systems are central to low power AI computing. AI computing is currently using massive amounts of power with an upwards trend. While the state-of-the-art material, $Ge_2Sb_2Te_5$ (a phase change chalcogenides), is still the favoured alloy, it is approaching its performance limits. For higher endurance and lower switching energy the development of current materials by sophisticated materials engineering in addition to research on new material compositions is urgently needed. Resistive switching materials are already commercialised for high performance SSD applications.

A memristor is a two-terminal variable resistor. Its resistance changes depending on the signals applied. Furthermore, resistance state is memorised in the OFF state i.e. when no signal is applied, i.e. non-volatile. Ideal materials candidates for memristors are a long retention characteristic, fast switching and an ultra-low power consumption. Some laboratory demonstrator memrisitive systems have the ability to support a multitude of resistive states.

Oxides

In the case of transition metal oxides the main bottle neck are limitations in the long-term stability of independent states. Resistive material random access memory is based on thermal, electrically or ionic stimulated changes of the resistance state of a metal-insulator-metal structure. [81] Material systems include (Ta_2O_5, HfO_2 and TiO_2 [82]). Self-learning spiking 8 × 8 crossbar array on a single chip with 64 synapses and 8 leaky integrate-and-fire neurons have been demonstrated. The synapses were built with non-volatile HfO-based synaptic drift memristors, and the 8 neurons with volatile silver-based diffusive

[81] R. Waser, et al., Nature Materials, 6, 833, (2007), https://doi.org/10.1038/nmat2023
[82] S. Stathopoulos, et al., Scientific Reports, 7, 17532, (2017), https://doi.org/10.1038/s41598-017-17785-1

memristors. [83] Resistive material technology is scalable beyond current CMOS technology[84]. HP envisions technology capabilities of 10 times the performance of NAND flash at 10 times less power consumption coupled with a longer life-time. Other companies which have invested in resistive random access memory are Panasonic, Toshiba and Micro. [84] A two neuron network consisting of Pt (10 nm)/TiO_2 (25nm)/Pt(10nm) demonstrating reversible unsupervised learning was demonstrated. [85] The key challenges are engineering materials to be highly uniform, with ability to scale. There are strong UK efforts in promoting this area including e.g. two Royal Academy Chairs in Emerging Technologies. Connection of efforts across the U.K. will strongly enhance the UK capability is this field.

Phase change materials

Phase change materials are more reliable than resistive materials but are also more affected by power and scalability issues [84]. Phase change materials have great potential for applications due to performance and cost benefits and could promise a universal storage class memory replacing SRAM, DRAM, NOR flash and NAND flash. Suppliers including Micron, IBM, Intel, Samsung and SK Hynix are pursuing development of the technology. However, an impact on the market is only envisioned when current 3D NAND flash has reached its 10 nm limit at the end of the decade. Phase change memory is based on a controlled temperature induced transition from a crystalline state to an amorphous state[83]. A successful demonstrator using one million phase change memory devices to perform high level computing was made doped $Ge_2Sb_2Te_2$ (d-GST) integrated into 90 nm CMOS technology. Energy efficiency of correlation computations of two order of magnitudes with the material used being doped $Ge_2Sb_2Te_5$ (d-GST) integrated into 90 nm CMOS technology. [86]

Ferroelectric materials

Non-volatile memory in which bits are stored in form of stable polarisation states can be achieve using ferroelectric materials. This is at an earlier stage of development than the aforementioned systems, with critical materials challenges being uniformity of operation and toxicity. Ferroelectric based memory enables low power performance and fast write speeds. Commercialised narrowly in 1990 using perovskite materials. However historically the severe challenge of integrating perovskite or layered perovskite ferroelectric materials into CMOS processes and realising three dimensional structures has hindered scaling below 100 nm and thus limited device density and market uptake. The discovery of hafnium oxide has changed this.

The most commonly studied material for memory applications is $PbZr_xTi_{1-x}O_3$ (PZT). PZT materials have a permanent polarization value of ~ 10–40 µC/cm^2, a permittivity of ~ 300–400, and a coercive field of ~ 50–70 kV/cm. However, fatigue problems set in if the active part of the device is coupled with a metallic contact such as Pt. A problem which can be avoid by using an oxide electrode. A leadfree alternative material system, $SrBi_2TaO_9$ reaches polarisation values of 5-10 µC/cm^2 with a coercive electric field of 30-50 kV/cm and does not suffer fatigue issues when paired with metal electrodes. On the other hand, $BiFeO_3$ has excellent ferroelectric properties, however it is almost a wide band gap semiconductor, rather than an insulator which is a disadvantage for applications. Furthermore, it is a complex material with non-uniformity issues. Its magnetic properties and potential for optoelectronics applications makes it attractive for other applications. As switching of a ferroelectric material requires a limited number of electrons to form a sizable energy barrier of 1 eV (1-10), ferroelectric materials which exhibit magnetic properties are key for very energy efficient

[83] Z. Wang, et al., Nature Electronics, 1, 137, (2018), https://doi.org/10.1038/s41928-018-0023-2
[84] Would the real flash storage successor please stand up? (2014), https://www.computerweekly.com/feature/Would-the-real-flash-storage-successor-please-stand-up?_ga=2.176675939.735273345.1592576100-881259463.1592576100
[85] A. Serb, et al., Nature communications, 7, 12611, (2016), https://doi.org/10.1038/ncomms12611
[86] A. Sebastian, et al., Nature Communications, 8, 1115, (2017), https://doi.org/10.1038/s41467-017-01481-9 ; I, Boybat, et al., Nature Communications, 5, 9, 2514, (2018), 10.1038/s41467-018-04933-y

hybrid applications where the polarisation induces a magnetisation reversal in a neighbouring ferromagnetic layer.

Due to the ability to grow ferroelectric thin films fluorite based ferroelectric materials such as Si doped HfO_2, undoped HfO_2 and solid solutions of HfO_2-ZrO_2 are of interest. They have already been used as dielectrics in CMOS technology and thus provide an excellent solution for next generation ferroelectric computing applications. However, reproducibility, wake-up effects, and cycling fatigue are problems as well as the large coercive field. Again, advanced materials control and engineering are challenges to addressed.

Piezoresistive Materials

Combining piezoeletric materials, materials in which a large volume change occurs under the application of an electric field, with a material which undergoes a hysteretic metal to insulator transition under pressure is a way to achieve a memristive transistor which is not subject to the voltage limits of a field effect transistor. [87] Gigahertz switching speeds can be achieved. [88] PZT is currently the dominant material with regards to achieving high strains and forces at a given voltage, however the relaxor material (1-x)[$Pb(Mg_{1/3}Nb_{2/3})O_3$] - x[$PbTiO_3$] (PMN-PT) is gaining traction [89] due to its high piezoelectric coefficient. Thin film growth development is focused on pulsed laser deposition growth due to its compatibility with CMOS technology. However, growth of single phase formation of perovskite PMN-PT systems is still a challenge. Advances towards growth on Si involve adding lattice matched substrates or template layers such as Si/STO/SRO or Si/TSZ/CeO/LNO. On the memristive side, a material with a large and hysteretic change in resistance is needed which is driven by a change in pressure. Proof of principle efforts are focused on rare earth monochalcogenides such as SmSe which are deposited using highly controlled state techniques. [90] An effect first observed in 1970. Switchable films can be achieved using sputtering methods. Piezoelectric memristors are at TRL 3-4 currently. Improvements need to be made on with regards to the materials interfaces and the quality of the piezoresistive material which will require modelling and a fast tracking of materials evaluation. A concern is also the incorporation of lead which may be problematic in the future due to its toxicity and life cycle concerns. However, innovation in other materials families such as Heusler compounds, other chalcogenides and oxides are promising and will be needed to be moved towards an industry prototype.

Magnetic materials

Magnetic random access memory (MRAM) is a technology which couples non-volatile bit retention, i.e. information is not lost when the device is switched off, with persistence, high endurance and low latencies. Information is stored in form of a two-state resistance level set by the relative orientation of magnetic layers within the device. [91] The first generation MRAM, toggle-MRAM, uses a magnetic field generated by an Oersted line to 'toggle' the magnetic state of one of the magnetic layers, the free layer. The magnetic easy axis is in plane in these devices. While it features virtually infinite endurance it is limited in scalability, bit density is limited currently to 32 Megabytes. [92] The second generation uses spin transfer torque to switch the free magnetic layer, i.e. electrical currents flowing though the device itself. This improves device scalability dramatically and 1 Gigabyte data densities are commercially available (Everspin [93]). While the switching latency is comparable in both products the significant improvement on energy per bit switched

[87] J. B. Chang, et al., Nanotechnology, 26, 37, (2015), https://iopscience.iop.org/article/10.1088/0957-4484/26/37/375201
[88] D. Newns, et al., J Appl. Phys, 111, 084509, (2012), https://doi.org/10.1063/1.4704391
[89] S.H. Baek, et al., Science, 334, 6058, (2011), DOI: 10.1126/science.1207186
[90] P.M. Solomon, et al., Nano Letters, 15, 2391, (2015), https://doi.org/10.1021/nl5046796
[91] IEEE International Roadmap for Devices and systems (2017 Edition)
[92] https://www.mram-info.com/ (last updated 2020), https://www.mram-info.com/stt-mram (last updated 2019)
[93] Everspin (2020), https://www.everspin.com/spin-transfer-torque-mram-technology

leads to a higher accessible bandwidth. Both toggle MRAM and STT-MRAM are commercial embedded system products. Advances in technology and materials design are moving towards perpendicularly magnetised MRAM device concepts driven by spin orbit torque which offers low energy consumption and an improved scalability. Further development efforts are made in areas such as voltage controlled [94] and four level resistance state[92] devices. State-of-the-art academic research demonstrated electrical switching of Magnetic tunnel junction in 0.2 ns in a 23 mT static in plane field using a combination of spin transfer torque and spin orbit torque at a critical switching energy of 0.5 pJ using a W (3.7 nm)/$Co_{20}Fe_{60}B_{20}$ (0.9 nm)/MgO (~1 nm)/$Co_{17.5}Fe_{52.5}B_{30}$ (1.1 nm)/W (0.3 nm)/Co (1.2 nm)/Ru (0.85 nm)/Co (0.6 nm)/Pt (0.8 nm)/[Co (0.3 nm)/Pt (0.8 nm)]$_6$ junction. [95]

Required activities	Implementation timescale*
Close collaboration between hardware development and software development	ST-LT
Achieve better understanding of fundamental physic and chemistry involved in the motion of ions, electrons and magnetic domains	ST-MT
Improvement of device performance through optimisation of materials properties.	ST
Improvement of interface control and design to enhance electrochemical processes, device and bit stability, improve switching characteristics and to reduce the overall power consumption, improve write-ability, yield and minimise writing energies	ST
Improve latency time and current densities	ST
Reduce memristor size while maintain performance	ST
Development of MTJ memory cells which are of comparative size to transistors while retaining stability against thermal fluctuations and which are addressable with very small current densities.	ST
Survey properties of less explored memristive materials such as antiferromagnetic phase memory.	ST
Translation of proof of principle multistate memristors to prototype	ST
Modelling across all length scales from atomistic, to device through to the architecture scale	ST
Development of benchmarking framework enabling a direct comparison between the different materials and technologies	ST
Development of selection criteria for materials discovery.	ST
Scale up of commercial production capabilities of materials as they become technologically ready	ST
Development of techniques for non-destructive probing of ferroelectric with high special and resolution	ST
Address scalability challenge of $PbZr_xTi_{1-x}O_3$ ferroelectric materials	MT
Development into lead free alternatives with improved performance	ST-MT
Address fatigue and coercive field challenge of fluorite based ferroelectric materials	MT
Catalogue matching materials properties to neuromorphic computing hardware and software	MT

[94] J. Liu, IMEC, (2020), https://techxplore.com/news/2020-06-fundamental-voltage-controlled-magnetic-ram.html
[95] E. Grimaldi, et al., Nature Nanotechnology, 15, 111, (2020), https://doi.org/10.1038/s41565-019-0607-7

Development of interface outputs and interconnects able to address large arrays of elements	MT
Optimisation of materials and device architecture to achieve noise suppression and optimise error correction	MT
Development of practicable co-processor or special purpose processor such as a neuromorphic processor	MT
Development of high quality, new piezoresistive composites materials. Using materials modelling.	MT-LT
Investigation into structure-functionality relationship of piezoelectric memristors	ST-MT
Scale down of piezoelectric memristor device size	ST-MT
Volume scale up and commercialisation.	LT
Achievement of cost reduction.	LT
Improvement of bit switching speeds through improved knowledge of dynamic effects	LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

The main **bottle necks** are lack of volume characterisation equipment, lack of large-scale (8'' inch wafer growth) compatible prototyping line and limited access to high end (single nm write-line, large wafer compatible) lithography tools.

Charge to Spin Current Conversion

In order to convert charge currents to spin currents, in order to manipulate a magnetic material, or to convert a spin current to a charge current, to sense a change in a magnetic material, requires materials with large spin orbit coupling. Conversion occurs either via the **Spin Hall effect** or the inverse **Spin Galvanic effect** (or Rashba Edelstein effect) in **Heavy metals** (e.g. Pt, [96] Ta, Ir, W)**, Topological oxides (**e.g. Bi_2O_3, [97] $SrIrO_3$, [98] $SrTiO_3/LaAlO_3$ [99]), **Topological materials and superlattices** (e.g. $Bi_{1.5}Sb_{0.5}Te_{1.7}Se_{1.3}$, [100] Bi_2Se_3, [101] α-Sn, [102] BiSb [103]), and **Two-dimensional transition metal dichalcogenides** (e.g. MoS_2, MX_2. [104]). Topological materials have great potential in spin based technologies, however, they are at the fundamental research level. Understanding their physics and materials processing needs fundamental development. Their potential lies in their linear dispersion which results in high mobility and low electrical losses. Furthermore, they can be used to carry dissipationless currents. Their potential in active parameter tunability and reconfigurability might open many new avenues for innovation.

Magnetoelectric Materials

An exceptionally energy efficient charge driven switching phenomena is based on charge switching a ferroelectric material which in turn switches a ferromagnet via magnetoelectric switching. This efficiency is due to the limited number of electrons which are required to form an energy barrier of 1 eV (1-10 electrons) in ferroelectric materials. Magnetoelectric materials can then induce a magnetisation reversal in a magnetic

[96] W. Zhang, et al., Nature Physics, 11, 496, (2015), https://doi.org/10.1038/nphys3304
[97] S. Karube, et al., Applied Physics Express, 9, 3, (2016), https://iopscience.iop.org/article/10.7567/APEX.9.033001/pdf
[98] D. Pesin, et al., Nat. Phys., 6, 376, (2010), https://doi.org/10.1038/nphys1606
[99] J. Varignon, et al., Nat. Phys., 14, 322, (2018), https://doi.org/10.1038/s41567-018-0112-1
[100] Y. Shiomi, et al., Phys. Rev. Lett., 113, 196601, (2014), https://doi.org/10.1103/PhysRevLett.113.196601
[101] Y. Fan, et al., Nat. Mater., 13, 699, (2014), https://doi.org/10.1038/nmat3973
[102] J.-C. Rojas-Sánchez, et al., Phys. Rev. Lett., 116, 096602, (2016),
[103] N. H. D Khang, et al., Nat. Mater., 17, 808, (2018), https://doi.org/10.1038/s41563-018-0137-y
[104] G. Wang, et al., Nat. Commun., 6, 10110, (2015), https://doi.org/10.1038/ncomms10110

material. The switch in the ferromagnet is then read back via spin to charge conversion through strong spin-charge coupling such as topological materials via the Rashba-Edelstein or topological two dimensional electron gases.[82]

Fundamentally, the challenges in spintronic devices for computing are efficient spin switching and effective spin detection additionally to the challenge of the interconnects. In order to tackle these challenges materials classes such as **Multiferroics** (e.g. $BiFeO_3$ [105], $LaBiFeO_3$, [106] $TbMnO_3$, [107] $LuFeO_3/LuFe_2O_4$ [108]), **Magnetostrictive materials:** (e.g. Fe_3Ga, [109] $Tb_xDy_{1-x}Fe_2$, FeRh [110]) and **Exchange bias** (e.g. Cr_2O_3, [111] Fe_2TeO_6 [112]),magnetically ordered materials such as **Ferromagnets** (e.g. Co, Fe, Ni, CoFe, NiFe, L10 alloys (e.g. FePt)) and **Heusler alloys** (e.g. X_2YZ and XYZ alloys (for example, Co_2FeAl, Mn_3Ga)) are of interest. Extensive materials engineering is needed to improve interfaces for integrated devices, operation temperature range, processing temperature compatibility and performance metrics to achieve the desired 1-10aJ performance and a device size of <10 nm. For example, spin to charge conversion efficiency (Inverse Edelstein length (IEL)) of 2.1 nm was demonstrated in (001) α-Sn (30 monolayers)/Ag (2 nm)/Fe (3 nm)/Au (2 nm) at room temperature. [113]

SPIN CURRENT DRIVEN DEVICES

Spintronic materials are a versatile group of materials suitable for hybrid non-volatile charge – spin architecture such as integrated MTJs for in memory computing or domain wall logic architectures or volatile nano-oscillator based (See previous sections).

Magnetic Racetrack Memory and Logic

Magnetic logic and racetrack memory embody fully solid state devices without any moving parts. Magnetic domains are moved by fields and or currents from stationary read and write elements. Both magnetic domain logic and racetrack memory are based on moving and manipulation of information, in form of magnetic domain walls, via spin polarised currents. Current state-of-the-art racetrack memories feature stacks of out of plane easy axis magnetic materials in form of ultrathin thin films interfaced with heavy metals heterostructure separated by non-magnetic spacer layers to control the long range dipolar interactions. . In systems consisting of TaN/Pt/Co/Ni/Co/Ru/Co/Ni/Co/TaN domain wall velocities can reach 750 m/s with driving currents of the order of 10^8 A/cm^2. [114] Alternative, using stacks based on ferrimagnetic materials such as AlO/TaN/Pt/Co/Gd/TaN enable additional tunability of parameters. Domain wall velocities reach 400 m/s at a current density of 10^8 A/cm^2. [115] State-of-the-art logic elements are demonstrated in out of plane easy axis materials which are dominated by interfacial driven effects such as Dzyaloshinskii-Moriya interactions and proximity effects created by interfacing ultrathin ferromagnetic thin films with heavy metals such as Pt/Co/AlO with single NOT gate operation in an area of 0.8x1 μm^2 at 20 pJ with a predicted down scaling of 20 aJ if a footprint of 10 x 10 nm^2 was achieved. [116]

Key materials parameters for success are perpendicular magnetic anisotropy, stable homochiral Néel domain walls, and large spin currents with controlled polarisation. The latter is created from a charge current through the spin Hall effects or interface effects such as the Rashba Edelstein effect and materials with large

[105] J. T. Heron, et al., Nature, 516, 370, (2014), https://doi.org/10.1038/nature14004
[106] Y. H. Chu, et al., Appl. Phys. Lett., 92, 102909, (2008), https://doi.org/10.1063/1.2897304
[107] T. Kimura, et al., Nature, 426, 55, (2003), https://doi.org/10.1038/nature02018
[108] J. A. Mundy, et al., Nature, 537, 523, (2016), https://doi.org/10.1038/nature19343
[109] N. Srisukhumbowornchai, et al., J. Appl. Phys., 90, 5680, (2001), https://doi.org/10.1063/1.1412840
[110] R. O. Cherifi, et al., Nat. Mater., 13, 345, (2014), https://doi.org/10.1038/nmat3870
[111] M. Street, et al. Appl. Phys. Lett., 104, 222402, (2014), dx. https://doi.org/10.1063/1.4880938
[112] J. Wang, et al., J. Phys. Condens. Mater., 26, 055012, (2014), doi:10.1088/0953-8984/26/5/055012
[113] J.C. Rojas-Sanchez, PRL., 116, 096602, (2016), https://doi.org/10.1103/PhysRevLett.116.096602
[114] S. Yang, et al., Nature Nanotechnology, 10, 221, (2015), https://doi.org/10.1038/nnano.2014.324
[115] R. Blaesing, et al., Nature Communications, 9, 4984, (2018), https://doi.org/10.1038/s41467-018-07373-w
[116] Z. Luo, Nature, 579, 214, (2020), https://doi.org/10.1038/s41586-020-2061-y

conversion efficiencies are of interest. Heavy metals such as Pt possess an efficiency in the order of 10-30%. Interfaces between heavy metals and Co induces the required perpendicular magnetic anisotropy and the Dzyaloshinskii-Moriya interaction which stabilises homochiral Néel domain walls.

INTERCONNECT MATERIALS

Interconnect materials include **noble metals**(e.g. Cu, Ag, Co, Al, SiO_2), **Metal–semiconductors** (e.g. Ru poly-Si, NiSi, CoSi, NiGe, TiSi), and **Interlayer dielectric** (e.g. SiN, SiCOH, polymers).

Spin current based interconnects are a potential candidate for low loss transmission of signals. While in theory spin currents propagate dissipationless and thus could lead to energy efficient interconnects. A key materials problem to address is spin scattering. The direction of the spins is not conserved i.e. the spins can flip their direction when undergoing a scattering event. This means frequent spin signal repeaters or regenerators would need to be added in order to transmit signal over the distances required on current chips.[80]

Superconductor Based Interconnects are very early in their development but promise zero resistance conduction of electrical signals. However, there are issues relating to operation temperature and functionality. Operation temperature lies 40 K below 300K and is an issue for domestic applications. Superconducting SQUID loops and superconducting interconnect have the potential to enable quantum computing and high power computing where low temperature operation is less of an issue and speed and low loss operation are of importance. Progress is being made in developing interfacing memory.

MAGNETO-OPTIC DEVICES

Linked to the optical computing themes are materials which change their order parameter through light bridging non-volatile computing, efficient switching and fast operation. Optical switching of magnetic materials is a process mediated by magnetic dichroism and/or thermal effects. Magnetisation reversal using light has unprecedentedly low heat load (<6 J cm^{-3}). [117] Interference enhanced absorption of light through microstructuring of the magnetic film was shown in GdFeCo. [118] Proof of concept, single-pulse switching of Co/Pt multilayers within a magnetic spin-valve structure ([Co/Pt]/Cu/GdFeCo) has been demonstrated. [119] Optically driven MTJs exhibit very fast switching speeds however they need high optical pulse energies to switch and due to growth incompatibilities the resulting poor MgO tunnel barrier leads to very low read out signals. GdFeCo is a good proof of principle material with switching times of 30 ps, however performance below 200 nm is impossible due to thermal stability issues.[119] Therefore, new materials for optical switching need to be developed. Other avenues combine optical switching with domain wall race track elements using Pt/Co/Gd heterostructures. [120] Ultrafast nonthermal photo-magnetic switching has been demonstrated in less than 20 ps at 20 aJ in a transparent YIG:Co film. [121]

It is also possible to optically generate a spin current, in contrast to switching a magnetic volume through light. For example, in GaAs through illumination of circular light a current of 200 pA/W was then generated at the surface of the topological insulator Bi_2Te_3 at 20K. [122]

[117] A. V. Kimel, et al., Nature Reviews Materials, 4, 189, (2019), https://doi.org/10.1038/s41578-019-0086-3
[118] M. Savoini, et al. Phys. Rev. B., 86, 140404(R), (2012), https://doi.org/10.1103/PhysRevB.86.140404
[119] S. Iihama, et al., Advanced Materials., 30, 51, (2018), https://doi.org/10.1002/adma.201804004
[120] M. L. M. Lalieu, et al., Nature Communications, 10, 110, (2019), https://doi.org/10.1038/s41467-018-08062-4
[121] A. Stupakiewicz, et al. Nature, 542, 71, (2017), https://doi.org/10.1038/nature20807
[122] Y.Q. Hiang, et al., Nature Communications, 8, 15401, (2017), https://doi.org/10.1038/ncomms15401

ANTIFERROMAGNETIC DEVICES

Antiferromagnets materials which possess magnetic order but do not have a net magnetisation, exhibit very fast dynamics and thus are of interest for fast computational approaches. Furthermore, they are sources and detectors of THz radiation. Antiferromagnetic materials open the door for faster operation for the same energy. Another advantage is their resilience to radiation and magnetic fields. [123] Electrical control of the orientation of the spins in CuMnAs on GaAs at THz frequency has been demonstrated. [124] CuMnAs can be growth with molecular beam epitaxy on GaP at temperatures between 220 and 230 ºC which is well below the CMOS circuit tolerance of 400 ºC.[123] As GaP is lattice matched to Si integration with CMOS is possible. Memory cell fabricated from Mn_2Au have been demonstrated. [125] Furthermore, optical writing is possible in CuMnAs nanostructures grown on GaP substrates with a single 100 fs laser pulse. [126] By realizing detection of the antiferromagnetic state via optical reflectivity the tool-box of electrical and optical writing and readout is achieved. Additionally to CuMnAs and Mn_2Au electrical control has also been shown in metallic MnN [127] and in insulating NiO [128] interfaced with a large spin–orbit coupling material such as Pt. [129] Other potential materials with room temperature antiferromagnetic order include IrMn, FeMn, Mn(II)Au, NiO, CoO, RuO_2 and several perovskites.

TWO DIMENSIONAL MATERIALS

The electronic properties of 2D materials encompass a wide range and includes semiconducting, insulating and metallic behaviour (including superconducting). They can have magnetic and ferroelectric phases. They are easily doped and hence can be designed to cover a broad range of parameters. Furthermore, two-dimensional transition metal dichalcogenides for examples are interesting candidates for spin to charge conversion.

Key limitations for widespread industrial uptake are that their scalability is highly material dependent and that some of the characteristics are so far only accessible at low temperatures. Insulating 2D materials so far can only be grown in atomic-sized flakes. However, for viable industry uptake large scale, good quality growth is necessary, and technologies will have to be developed towards this goal. The creation of heterostructures of 2D materials allows a flexible tuning of properties. Dry transfer techniques are crucial tool kits for laboratory based proof of principle device engineering. Reliable heterostructure development requires O_2 free atmosphere or immediate passivation of the top layer to prevent device breakdown. Some heterostructures can be drawn by chemical bath deposition. Industry manufacturing requires integration of different materials, including integration with Si. Industrial uptake of 2D materials so far is limited to passive thermal management.

Magnetic two-dimensional systems are interesting candidates for the study of low-dimensional magnetic behaviour. Transition metal phosphorus trisulfide (or thiophosphate), TMPS3, is an example which can host several transition metals such as Mn, Fe, Co, Ni, Zn and Cd, at the TM site and thus gives access to a fast variety of possible properties. It is a little explored field which has potential for many novel fundamental

[123] K. Olejník, et al., Nature Communications, 8, 15434, (2017), https://doi.org/10.1038/ncomms15434
[124] K. Olejník, et al., Science Advances, 4, 3 (2018), DOI: 10.1126/sciadv.aar3566
[125] S. Y. Bodnar, et al., Nature Communications, 9, 348, (2018), https://doi.org/10.1038/s41467-017-02780-x
[126] K. Kaspar, et al., preprint (2019), https://arxiv.org/abs/1909.09071
[127] M. Dunz, et al., preprint (2019), http://arxiv.org/pdf/1907.02386.pdf
[128] T. Moriyama, et al., Sci. Rep. 8, 14167, (2018), https://doi.org/10.1038/s41598-018-32508-w
[129] J. Shi, et al., Nature Electronics, 3, 92, (2020), https://doi.org/10.1038/s41928-020-0367-2

insights. [130] With new physical phenomena one expects a substantial shift in our ability to control and investigate nanoscale phases. [131] The current fabrication method via exfoliation is a drawback for commercialisation. Other growth methods need to be developed. Other techniques can produce magnetic monolayer such as chemical vapour deposition and molecular beam epitaxy. Most of the magnetic van der Waal materials are layered, cleavable transition-metal chalcogenides and halides. As such they are usually comprised of a layer of metal ions between layers of chalcogens or halides. Diverse magnetic and electronic properties have been found in these systems which include ferromagnetic semiconductors, such as $Cr_2(Si,Ge)_2Te_6$ and MSe_2 (M = V, Mn), itinerant ferromagnets, such as Fe_3GeTe_2, and insulating antiferromagnets (AFMs), such as MPX_3 materials where M refers to the transition metal and X to S or Se. Materials development challenges to overcome are materials discover, growth, stability, exposure to Oxygen and reproducibility.

ORGANIC AND MOLECULAR SPINTRONIC MATERIALS

The main advantage of organic materials in general is the ease by which they can be processed. They have a low thermal budget. However, the challenge with the performance of organic materials lies in their low operational frequency which is a limiting factor for some applications. The main processing issues are stability, printability and reconfigurability, i.e. the integration of organics with inorganic contacts as well as the diffusion that can occur in the organic material itself. A crucial engineering step in organics is encapsulation, ensuring oxygen does not enter the system. Furthermore, the management of lattice vibrations, phonons, is crucial which needs to be addressed for higher operation power and heat dissipation (in the spintronics space organic materials are of interest as biosensors).

Growth of nanocarbon and molecular thin films

Over the last decade, there has been a concerted effort in the growth of high-quality organic and fullerene based, resilient thin films using techniques that are CMOS-compatible. High vacuum thermal evaporation, together with spin coating and electro-spray, offer alternatives to grow hybrid devices containing molecules and carbon-based materials (e.g. Phthalocyanines α-CoPc, carbon based molecules). These layers can be the active component of the device or they can be used to tune the electronic properties of adjacent layers, such as ultra-thin metals or 2D materials, via charge transfer, interface orbital hybridisation and/or gate voltages.

Carbon based molecules

Carbon-based molecules offer a sustainable alternative to heavy metals, doped semiconductors and rare earths. These abundant, light, eco-friendly materials are of interest due to the small spin orbit coupling of light elements and a lack of hyperfine interaction in 12C leading to long spin coherence and diffusion times i.e. the interval before an electron spin changes its direction. However, molecular electronics and spintronics has faced challenges with replicating effects seen in conventional crystalline devices due to bad reproducibility, low carrier mobility and degradation. Nevertheless, molecular spintronics has remained a fruitful field of research because of the various novel behaviours and effects which are unique to molecular systems. In particular, interfaces, that can be exploited in multifunctional devices are of interest. [132] Molecular nanostructures can also be used to build spintronic devices or in spin-voltage conversion structures via the inverse spin Hall effect. [133, 134] There has been a concerted effort to comprehend the

[130] Je-Geun Park, J. Phys.: Condens. Matter, 28, 301001, (2016), https://iopscience.iop.org/article/10.1088/0953-8984/28/30/301001/meta
[131] K. S. Burch, et al., Nature, 563, 47, (2018), DOI: 10.1038/s41586-018-0631-z
[132] M. Cinchetti, et al., Nature Materials, 16, 507, (2017), https://doi.org/10.1038/nmat4902
[133] K. Ando, et al., Nature Materials, 12, 622, (2013), https://doi.org/10.1038/nmat3634
[134] D. Sun, et al., Nature Materials, 15, 863, (2016), https://doi.org/10.1038/nmat4618

complex spin-dependent charge interactions between molecules and metals, in particular the formation of spin-polarised interfaces and tunable surface states, where molecular materials offer unique behaviour and tunability that can be exploited to produce multifunctional devices via charge transfer and hybridisation when in contact with other materials. [135], [136] Charge transfer can take place innately due to band mismatching or be prompted by gate fields or optical irradiation. In parallel with these studies, observation and predictions have been made that molecular hybridization can drastically modify the spin-texture of surface states in materials used for spin-charge conversion via spin orbit coupling or in spin capacitors. [137], [138], [139]

Molecular layers can control and balance interactions in designer magnets. It has been observed that anti-ferromagnetic interface states form between a variety of organic molecules and Co or Fe films, resulting in changes to their magnetic anisotropy. [140], [141], [142] High coercivity magnets are an important resource for renewable energy, electric vehicles and memory technologies. Most hard magnetic materials incorporate rare-earths such as neodymium and samarium, but concerns about the environmental impact and supply stability of these materials is prompting research into alternatives. A much less explored possibility in the Long-Term could be the use of molecular materials to enhance the coercivity of 3D transition metal-based ferromagnets without rare-earths.

[135] F. Al Ma'Mari, et al., Nature, 524, 69, (2015), https://doi.org/10.1038/nature14621
[136] K.V. Raman, et al., Nature 493, 509, (2013), https://doi.org/10.1038/nature11719
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[138] S. Jakobs, Nano Lett. 15, 9, 6022, (2015), https://doi.org/10.1021/acs.nanolett.5b02213
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[140] M. Gruber, et al., Nature Materials 14, 981, (2015), https://doi.org/10.1038/nmat4361
[141] K. Bairagi, et al., Phys. Rev. Lett. 114, 247203, (2015), https://doi.org/10.1103/PhysRevLett.114.247203
[142] T. Moorsom, et al., Phys. Rev. B., 101, 060408(R), (2020), https://doi.org/10.1103/PhysRevB.101.060408

SPINTRONICS ON FLEXIBLE SUBSTRATES AND SENSORS

Implementation of sensors on flexible substrates is of importance to enable operation on soft and elastic surfaces such as artificial electronic skin applications and for smart packaging. Furthermore, electric and magnetic field sensors are a key component of robotic systems which enable positioning and orientation in space. The challenge lies in developing a robust device while keeping costs down through simplify the processing and device structures (e.g. reducing the number of layers in junctions), whilst matching the performance benchmarks necessary for the application. Recent times have seen advances such in the technology producing sensor systems consisting of 2x4 array of giant magnetoresistance magnetic sensors fabricated from permalloy ($Fe_{81}Ni_{19}$) Cu multilayers, an organic bootstrap shift register which controls the sensor matrix and organic signal amplifiers is underway. [143], [144] Fabrication of CoFeB/MgO tunnel junctions directly on flexible polyimide substrates with a 100% tunnel magneto resistance ratio has been demonstrated [145] as well as sensors based on heteroepitaxic Fe_3O_4/Muscovite films on flexible substrates. [146]

Required activities	Implementation timescale*
Development of spintronic based devices via light or currents avoiding external magnetic field routines.	ST
Integrate readout mechanisms suitable for an integrated on-chip readout.	ST
Integration of magnetic out of plane random access memory (reference to in memory computing) for non-volatile processing and logic	ST
Development of viable replacement for Pt in strong perpendicular magnetic anisotropy materials systems and SOT based devices	ST
Integration of heat-assisted and microwave assisted magnetic recording for lower energy and higher density data storage	ST
Optimisation of Heat assisted recording addressing issues with optics and transducers	ST
Integration of semiconductor spintronics devices which are compatible with silicon fabrication for non-volatile logic and electromagnetic sensing.	ST
Development of spintronics devices on flexible substrates for IoT and sensing applications.	ST
Fundamental research into spin injection from and to topological Insulator and 2D interfaces for dissipationless currents especially with the long-term goal of extending the operational temperature to room temperature.	ST
Fundamental research into improving operational temperature and efficiency of spin current generation as well as into increasing the length of scatter free spin current transmission.	ST
Fundamental research into topological insulators growth to improve yield and quality	ST
Fundamental research into spin topological materials and materials properties	ST
Fundamental development of toolboxes to grow, manipulated and read out antiferromagnetic based devices	ST
Direct benchmarking of antiferromagnetic based devices against existing technology	ST

[143] Leibniz Institute for Solid State and Materials Research (2020), https://techxplore.com/news/2020-01-fully-flexible-electronics-magnetic-sensors.html
[144] M. Kondo, et al. Science Advances, 6, 4, (2020), DOI: 10.1126/sciadv.aay6094
[145] S. Ota, et al., Applied Physics Express, 12 053001, (2019), https://iopscience.iop.org/article/10.7567/1882-0786/ab0dca
[146] P-C Wu, et al., Asc Appl. Mater Interfaces, 8, 49, 33794, (2016), https://doi.org/10.1021/acsami.6b11610

Optimisation of antiferromagnetic materials properties such as operational temperature range and bit lifetime.	ST
Fundamental antiferromagnetic materials discover.	ST
Translation of proof of principle into a prototype benchmarking device e.g. an antiferromagnets in-memory element	ST
Equipment development to improve aspects such as imaging of antiferromagnetic domains, time resolution, special resolution. Development of high frequency characterisation tools	ST
Fundamental development into modelling of antiferromagnetic modelling across all length scales and into the dynamic behaviour at high frequencies	ST
Fundamental research into antiferromagnets as THz source and detectors	ST
Linkage of spintronics and terahertz community	ST
Fundamental research and development into modelling including DFT and micromagnetic simulation, development especially in the region of antiferromagnetic behaviour and dynamics in the THz regime.	ST
Fundamental research into artificial multiferroics.	ST
Fundamental research into the development of designer materials - using known components e.g. L10 alloys	ST
Fundamental research into heterostructures of metals and oxides for memristive and racetrack applications.	ST
Fundamental research into oxide/molecular interfaces to address abundance and scarcity of materials	ST
Fundamental research into metal/molecular compounds to address abundance and scarcity of materials	ST
Close collaboration between material modelling, growth, characterisation and device fabrication for organic and molecular spintronics materials.	ST
Improvement of the reproducibility of device performance of organic and molecular spintronics materials.	ST
Understanding correlation between processing and the structure of the organic material.	ST
Improvements to wafer-scale growth and nanofabrication of organic and molecular spintronics materials.	ST
Coordination of academic research with links to industry to explore a wide variety of solutions with the goal to identify targets and materials and devices with commercialisation potential	ST
Race-track memory architecture – beating domain size limit and going into vertical integration e.g. 3D elements, controlling elements	ST-MT
Fundamental research into dynamic behaviour of magnetoelectric/ferroelectric switching. Exploration of possible materials combinations for practical magnetoelectric switching and read out	ST-MT
Unravel the fundamental interactions that control spin physics at molecular interfaces	ST-MT
Fundamental research into magnetic and multiferroic 2D van der Waals structures	ST-LT
Fundamental research into molecular based spintronics device development	ST-LT
Exploration of tunability of properties by interface hybridisation of organic and molecular spintronics materials	ST-LT

Proof of principal of Hybrid computing including optically switched magnetic materials (link to hybrid and optical computing section)	MT
Spintronic THz frequency sources and sensors for fast and efficient computing and communications	MT
Proof of principle demonstration of working magnetic and spin texture devices based on topological spin states such as skyrmions and synthetic antiferromagnetic domain wall logic.	MT
Demonstration of spintronic devices with an active magnetic/multiferroic device with a volume of less than 1,000 nm^3 and a stability of 100kBT switchable with an energy of 1 aJ ~ 6.25 eV ~ 240kT	MT
Demonstration of low stochastic errors in switching reproducibility and fatigue of ferroelectric, magnetic and multiferroic materials.	MT
Development of on chip magnet/ferroelectric state detection mechanism with high read-out voltage > 100 mV	MT
Development of material with large inverse spin–orbit effects, such as the spin galvanic effect/Edelstein effect how to achieve λ_{IREE} > 10 nm	MT
Actively tuneable spin-orbit coupling materials	MT
Development of material architectures and device concepts for spin topological materials	MT
Solve interconnect issue of topological materials	MT
Development of actively tuneable material systems e.g. Rashba effect, permeability, permittivity, etc.	MT
Magnetic heterostructures for thermoelectric applications	MT
Demonstration of effective transduction of a spintronic/multiferroic state to a photonic state (and vice versa) enabling long distance interconnects (> 100 μ m)	MT
Demonstration of stochastic switches (spin/ferroelectric) operating near practical thermodynamic conditions in a computing architecture	MT
Optimisation of microwave assisted recording through engineering of spin-transfer oscillators	MT
Optimisation of materials properties and growth and interfaces of antiferromagnetic devices	MT
Addressing issues with interfacing organic and molecular spintronics materials with standard semiconducting devices.	MT
Agreement of standards for device performance and methodologies	MT
Connection with industry for real applications of molecular materials within current processes	MT
Material modelling and screening methods in realistic environments including defects, applied currents/voltages and magnetic fields	MT
Optimisation of organic and molecular spintronics materials and device architecture to achieve noise suppression and optimise error correction	MT
Improvement of use of recyclable and sustainable materials	MT
Equipment development to improve aspects such as imaging of antiferromagnetic domains, time resolution, special resolution. Development of high frequency characterisation tools	MT
Achieve integration into CMOS of antiferromagnetic materials based devices.	MT
Development of antiferromagnetic materials growth using CMOS compatible techniques	MT
Development of large antiferromagnet based device	MT

Industry engagement to evaluate device performance critically with attention to scale-up and integration possibilities	MT
Development of the 2D materials catalogue	MT
2D materials to be used for active thermal management	MT
Development of 2D chalcogenides and molecules and 2D materials processing techniques that are CMOS compatible.	MT
Exploitation of interface properties and control (hybrid materials)	MT
Overcome challenges in spin amplification devices, spin repeaters on a 10nm or sub-10nm length scale	MT-LT
Addressing of the interfaces challenge and spin de-coherence and scattering	MT-LT
Demonstration of optically switched materials at THz frequency, natural materials candidate are antiferromagnets	MT-LT
Continue to address challenges in growth and application of topological materials systems	LT
Charge less integrated memory and logic for ultra-low energy consumption using spin waves eliminating Joule heating losses (devices operating close to or at the fundamental thermodynamic energy limit, the landau limit). Paving the way to devices operating close to the Landau limit.	LT
Integration of magnetic, ferroelectric and multiferroic materials into the back-end of the CMOS i.e. demonstration of materials grow on an amorphous layers and at suitable temperatures at temperatures below 400 C.	LT
Demonstrate 10 billion functional spin based switches per chip utilize the extreme size, logic efficiency and three dimensional integration	LT
Development of emerging magnetic properties from non-magnetic bulk materials.	LT
Achieving permanent and tunable magnetism without using rare earth material	LT
Hybridisation of different materials systems achieving superior performance	LT
Development of single molecule properties for single molecule memory	LT
Development of permanent and tunable magnets without using rare earth materials	LT
** ST = Short-Term (now-2030), MT = Medium-Term (2030-2040), LT = Long-Term (2040-2050)*	

The main **bottlenecks** are poor reproducibility, degradation and lack of established standards for organic and molecular materials for spintronics which leads to problems in translating lab-based single (or small volume) device research into industrial scale operation as well as the policy changes required to establish industrial interest in carbon-based materials to balance costs in production changes and investment in research in these materials. There are additional issues with lack of universal, established nanofabrication protocols for chemically sensitive organic materials, lack of intermediate scale test line to trial new materials and concepts, and poor of communication between industry and academia.

UK CAPABILITIES

The UK has a large and very active spintronics, ferroelectrics, resistive memory and photonics community. With a wide set of academic laboratory-based tool kit. Furthermore, cleanroom facilities and lithography tools are available for small scale laboratory-based proof of principle devices (e.g. University of Southampton, University of Glasgow, University of Cambridge, LCN, University of Leeds, University of Manchester, etc.). The same holds for growth and deposition tools. However, commercial materials manufacturing and design

knowhow for computing is less abundant. Seagate Technology holds the largest share in the UKs semiconductor and components for electronic applications in the UK, specialising in magnetic information storage and read and write heads. In general, there is a trend towards fabless production or outsourcing of production and manufacturing in countries with cheaper labour costs. However, the UK is well situated to drive the development and innovation to the industrial prototype level and needs to be ready to capitalise on the knowhow generated on the way.

UK COMMUNITY RECOMMENDATIONS

It is widely recognised there is a strong UK academic base with great capacity for long term innovations in the development of new materials and device concepts. However, the high initial cost associated with CMOS fabrication lines, and the current trend to outsource production to other countries, has caused a void with respect to relevant industry and supply chains within the UK. As a consequence, full scale up of new concepts within the UK is extremely difficult at present, and a paradigm shift in approach is needed.

The UK community must focus on determining and understanding the current societal challenges. It then needs to find the necessary solutions, bringing together academic institutions, catapults and industry encompassing scientists, engineers and business economists. To enable this, the community recommends that a new Centre is established (either co-located or distributed, but with a clear central hub) to develop 'More-than-Moore' materials and device concepts focusing on low loss electronics. This Centre would support the prioritisation of technical opportunities and identify the tangible benefits, including addressable markets and revenue streams to build a balanced UK portfolio. It would be able to appraise critically opportunities for the UK including scenario planning, from an independent perspective, and identify where targeted investment would unlock transformative opportunities for UK business.

It is essential that the effective teams are established to build on the UK academic strengths and take laboratory curiosities to demonstrator devices and manufacture. This requires coordination of efforts on a national level as well as collaboration internationally. It is also essential that the UK invests in equipment to improve materials growth, enabling atom to atom control, single crystal thin film growth, precise interface control, thickness control, and the growth of variety of different materials within the same system. This must be accompanied by the design of new tool sets for atomistic control. The development of internal telemetry to monitor directly gas species (e.g. ion energies, reactive and inert species) would also support the scale-up of processing tools from research to manufacture and enable co-processing of disparate materials in common pilot line tools.

Parallel investments will be required to deliver high spatial and/or temporal resolution techniques that enable characterisation of materials properties and mapping. This includes the development of non-destructive characterisation techniques and improvements of the lithography capabilities across the UK to <10nm. Investment is also need to maintain and enhance state-of-the facilities such as: low noise voltage and current measurements (including cryogenic capabilities), magnetometry, electron and magnetotransport apparatus, atomic scale microscopy, SEM and TEM that avoid chemical damage and degradation during the measurement, characterisation and imaging including interface sensitive techniques (SuperSTEM, TEM, SPM, XRD FMR, ARPES (especially for development of nanostructure capabilities), THz spectroscopy, nanoscale materials tomography and functional property mapping. There is also a need for vacuum suitcase technologies to enable samples to be moved between different processing and analytical tools without contamination and degradation. This needs to be supported by a central equipment and

technology catalogue to capitalise on the UK capabilities that are distributed between academic and industrial institutions, with easy, transparent access to the community.

For development of new computing architectures, discovery, optimisation and development of materials is essential, both experimentally and theoretically, through modelling across all length scales spanning the atomistic, materials, device, architecture and the system level. An AI approach to materials discovery would identify suitable next generation materials for non von Neumann computing, especially in the area of heterostructures and antiferromagnetic materials. A key parameter that need to be considered right at the outset of the materials discovery process are the abundance, recyclability and ease of sourcing of the materials, as well as toxicity and life cycle analysis.

Currently, there is a bottle neck in the transition from the research environment to commercialisation. A significant limitation is the inability to test new technology for compatibility with large scale production lines. This needs to be addressed. A greater transfer of knowledge between industry and academic stakeholders is required from the outset, with more incentives for industry to participate in discovery-led and low TRL research. Innovation from the academic community must then be efficiently translated and tested on intermediate level pilot lines, prior to evaluation for manufacture.

CONCLUSIONS, RECOMMENDATIONS AND KEY MESSAGES

There are significant opportunities for the UK to undertake transformative programmes of materials research and development that reduce energy consumption in electronic components and systems. By bringing together academia and industry, it will be possible to meet society's ever-increasing demands for more sophisticated electronics, whilst reducing its overall carbon footprint. This will directly support inward industrial investment, capitalise on the UK's strengths in advanced materials, and enable the UK to be an internationally leading innovator in the device supply chain, providing sovereign capability.

Strategic investments into UK prototyping and pilot plants, combined with high throughput device testing capabilities, will enable scale-up of devices from research to wafer-scale fabrication. Centres for growth, fabrication and characterisation are needed to develop new materials to the point of proof-of-principle and reflect optimal strategies for addressing the scale-up of the diverse range of materials needed to develop future electronic devices. Supporting and implementing new material discovery approaches was identified as a key enabler to accelerate material development, e.g. machine learning (AI) approaches, together with simulation and modelling across different length scales. To achieve tangible outcomes by 2050, a clear collaborative dialogue between UK-wide academia and industry needs to be established from the outset of the materials development process, with a focus on long-term commercial exploitation.

Key findings include the need for:

- Investment to support UK prototyping/pilot-plant scaling of devices from research to wafer-scale fabrication and manufacture, including validation and testing; this provides a supply chain to test and translate new ideas.
- Investment in a network of state-of-the-art 'fab-of-the-future' centres, accessible to the whole UK, encompassing the design, growth and fabrication of new materials. This would be supported by UK Centres in *Materials Replacement & Recycling*, *High-frequency Devices*, and *High-throughput Testing,* each underpinned by world-class scientists and engineers, with dedicated specialist technical staffing
- Development of techniques to effectively and efficiently embed new materials into high performance, energy efficient devices, including interfacing with the external environment.
- Establishment of big data and machine learning (AI) approaches to materials discovery (Materials 4.0) and advancing the understanding of interfacial properties (Interface 4.0), supported by accessible materials databases, and simulation and modelling development across the length scales – from atoms to devices.
- Investment to support the development of new computing architectures, and next generation wide-bandgap semiconductors for power electronics.
- Funding approaches to support UK-wide collaborations between academia and Industry.
- Investments and incentives for industry to undertake research, and lead and develop exploitation strategies.
- Influencing policy, including setting power consumption targets, supporting the circular economy through end of life considerations, and removing reliance on lifecycle supply-constrained materials

In summary a crucial pathway towards achieving commercially viable products is a close collaboration between industry and academia from initial materials discovery through to materials optimisation, prototype demonstration, scale-up and manufacture. This must be guided by clear and transparent approaches to prioritise the opportunities which will have the greatest positive impact on UK industry. Finally, establishing

policies that set power consumption targets, and support the circular economy through to end of life considerations, will be a critical factor in establishing an environment where the UK takes a leading position and becomes the place for investment for the future development of *low loss electronics*.

Addressing the government's net zero targets necessitates the development of completely new device concepts and architectures. This requires focused interventions now if solutions are to be ready to meet the ambitious 2050 targets.

APPENDICES

APPENDIX I: WORKSHOP DETAILS

The workshops were commissioned by the Henry Royce Institute and delivered by IfM Education and Consultancy Services Limited.

Workshop Methodology

The roadmapping workshop methodology consisted of three parts: design, the workshops, and reporting of the workshop outcomes.

Workshop Design

During the design phase, the following activities took place:

- Discussing and designing in detail the workshop methodology and process. The workshop used the **S-Plan** framework developed by the IfM over several years. [147, 148, 149] The framework has been configured to help universities and research organisations align their research activities with industry needs, supporting decision-making and action;
- Designing the templates necessary to support the workshop activities;
- Agree on the detailed workshop agenda;
- Agree to the desired workshop outputs.

Workshops Description

The roadmapping workshop process brought together around 30 participants from the research community and industry and had the following structure:

- First Session (WS1)
    - To **review** the delegate and IOP survey content submitted so far.
    - Identify and fill in any **gaps.**
    - Review and feedback.
- Second Session (WS2)
- To **discuss** topics that that would be appropriate (relevant, impactful and that experts can meaningfully contribute to)
- To **select** the priority ideas for topic roadmapping
- To set up the **working groups** that will be exploring each idea in Workshop 3
- Third Session (WS3)
    - To **explore** selected **key priority** materials for low loss electronics

[147] http://www3.eng.cam.ac.uk/research_db/publications/rp108
[148] R. Phaal, et al., Research Technology Management, 47, 2, 26, (2004)
[149] R. Phaal, et al., Engineering Management Journal, 19, 1, 16, (2007)

- To **scope** each priority idea
- To map **the research and development path** and required resources
- To describe **the expected deployment** and required technological and commercial enablers

- Fourth Sessions (WS4)

  Additional workshops were held to encourage a wider community to be built and consulted. The format of the session was as per WS3.

- To **explore** selected **key priority** materials for low loss electronics
- To **scope** each priority idea
- To map **the research and development path** and required resources
- To describe **the expected deployment** and required technological and commercial enablers

Indicative Workshop Agenda

Session 1	
10:00 – 10:05	Welcome from HRI
10:05 – 10:15	Introductions, objectives and workshop 1 process
10:20 – 10:30	Discussing the content collected so far (data provenance and review process)
10:30 – 11:30	Review pre-work and identify gaps for materials and systems (in small groups)
11:30 – 11:55	Feedback review of group review (5 minutes presentation)
11:55 – 12:00	Wrap-up and process feedback

Session 2	
09:00 – 09:10	Introductions, objectives and workshop 2 process
09:10 – 09:25	Review the short, medium and long term prioritisation results in groups
09:25 – 09:35	Feedback of review discussion (5 minutes presentation)
09:35 – 09:55	Set up the working groups for exploring the different topics
09:55 – 10:00	Wrap-up and process feedback
Sessions 3 and 4	
13:00 – 13:10	Introductions, objectives and workshop 3process
13:10 – 14:25	Exploration of selected topics
14:25 – 14:55	Presentation and review
14:55 – 15:00	Wrap-up and feedback

Dates of Workshops

First Session: 30 March 2020,
Second Session: 3 April 2020,
Third Session: 3 April 2020,
Fourth Sessions: 19 – 22 May 2020

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